23 µW 8.9-effective number of bit 1.1 MS/s successive approximation register analog-to-digital converter with an energy-efficient digital-to-analog converter switching scheme

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Abstract: This study presents a successive approximation register analog-to-digital converter with an energy-efficient switching scheme. A split-most significant bit capacitor array is used with a least significant bit-down switching scheme. Compared with the conventional binary-weighted capacitor array, it reduces the area and average switching energy by 50 and 87% under the same unit capacitor. Moreover, capacitor matching requirement is relaxed by 75%. A prototype design was fabricated in a 0.13 µm complementary metal oxide semiconductor process. It consumes 23.2 µW under 1 V analog supply and 0.5 V digital supply. Measured results show a peak signal-to-distortion-and-noise ratio of 55.2 dB and an effective resolution bandwidth up to 1.1 MHz when it operates at 1.1 MS/s. Its figure-of-merit is 44.1 fJ/conversion-step.

1 Introduction

With the permeation of wireless sensor networks and handheld or wearable devices with built-in sensors, compact and low-power analog-to-digital converters (ADCs) with medium bandwidth are highly demanded [1–5]. The successive approximation register (SAR) ADC earned its dominance in this field of applications because of its area and power efficiency resulting from its nature of binary search algorithm [6]. An SAR ADC normally consists of a digital controller, a comparator and a capacitative digital-to-analog converter (CDAC). It requires the least active circuits and avoids the use of amplifiers, which increasingly become a bottleneck in scaled complementary metal oxide semiconductor (CMOS) technologies because of the decline of intrinsic gain in short channel length transistors. When a dynamic comparator (without pre-amplification) is used, the power dissipation of the SAR ADC is partly because of switching activities and partly because of leakages (which is more important in lower speed applications) [7]

\[ P_{\text{ADC}} \approx \alpha CV^2f_{\text{clk}} + P_{\text{leakage}} \]  

(1)

Intuitively, reducing the capacitance lowers the power dissipation. Digital circuits naturally benefit from smaller device and wire parasitic capacitances in scaled CMOS. The comparator’s power does not scale as in digital circuits [8] because it has to drive a large load capacitance for noise immunity, unless special techniques such as data-driven noise-reduction method [9] are applied. The switching power in the CDAC can be lowered by using a smaller unit capacitor [9]. However, the minimum value of the unit capacitor is commonly set by matching [10], noise requirement or process limitation. Decreasing the supply voltage saves some power at the cost of reduced analog signal swings. Lastly, the CDAC structure and switching scheme have a great impact on its switching power consumption. The split-capacitor [11], energy saving [12], set-to-down [13] and \( V_{\text{cm}} \)-based [14] CDACs reduce the average switching energy by 37, 56, 81 and 87%, respectively, compared with the CDAC using the conventional binary-weighted capacitor array (BWA) with the same unit capacitor. However, the set-to-down encounters the problem of common-mode (CM) voltage variation at the comparator’s inputs; the \( V_{\text{cm}} \)-based CDAC needs an extra reference voltage \( V_{\text{cm}} \) and the buffer driving it. To overcome these minor problems, a CDAC switching concept, namely ‘split-most significant bit (MSB) with least significant bit (LSB) down’ is reported in [15, 16] [The group of researchers of [16] developed a similar technique. Our work was done independently before the publication of [16]], which in theory saves the CDAC switching power and area by 87 and 50%, respectively, compared with the BWA CDAC with no side effects. In this work, an SAR ADC adopting this concept is designed in a 0.13 µm process. It measures an 8.9-effective number of bits (ENOBs) at 1.1 MS/s, consuming 23.2 µW.

2 SAR ADC architecture

2.1 Architecture

Fig. 1 shows the SAR ADC architecture, which is fully differential in order to suppress substrate, supply and other CM noise. It consists of four blocks, namely, CDAC, comparator, digital controller (operating from 0.5 V) and level shifter between the controller and the rest of the ADC (operating from 1 V). The capacitances of the \( N \)-bit ADC are given in the following equation

\[ C_i = C_{2,i} = 2^{N-i}C_0, \quad i \in \{3, \ldots, N\} \]  

(2)

where \( C_0 \) (and \( C_{2,0} \)) is the unit capacitor. The total capacitance in a split-MSB array is \( 2^N - 2C_0 \). The subscript ‘2’ indicates those capacitors are the split ones of the largest capacitor \( C_2 \) in the conventional BWA.

The operation of the ADC is described as follows. Consider the positive half circuit. During the sampling phase switches \( S_{\text{L}} \) close, the input \( V_{\text{IN}} \) is sampled on the top plate of all the CDAC capacitors in the half circuit. The bottom plates of the split-MSB capacitors are connected to \( V_{\text{cm}} \), whereas the others are connected to ground. Top plate sampling is employed here for better energy efficiency because the MSB can be resolved right after the sampling without switching any capacitors. The other half circuit works on \( V_{\text{IN}} \) in the same manner.

After sampling, the inputs are held by opening switches \( S_{\text{H}} \). The comparator outputs \( b_1 = 1 \) (\( b_1 \) stands for MSB here) if \( V_{\text{DACP}} > V_{\text{DACN}} \); otherwise \( b_1 = 0 \). In the next clock phase, if \( b_1 = 1 \), the...
largest split-MSB capacitor $C_{2,3} = 2^{N-3}C_0$ in the positive array switches from $V_{\text{ref}}$ to ground to decrease $V_{\text{DACP}}$ by $V_{\text{ref}}/4$. Simultaneously, $C_3$ (also $= 2^{N-3}C_0$) in the main array of the negative half circuit switches from ground to $V_{\text{ref}}$ to increase $V_{\text{DACN}}$ by $V_{\text{ref}}/4$. The opposite takes place if $b_1 = 0$. Then $V_{\text{DACP}}$ is compared with $V_{\text{DACN}}$ to resolve the second MSB, $b_2$. The process repeats until the second LSB ($b_{N-1}$) is resolved as illustrated in an example in Fig. 2.

To resolve the LSB ($b_{N}$), only one unit capacitor ($C_{2,3}$) in the split-MSB array, in either positive or negative half circuit (depending on $b_{N-1}$), switches from $V_{\text{ref}}$ to ground to change ($V_{\text{DACP}} - V_{\text{DACN}}$) by a positive or negative amount of $V_{\text{ref}}/2^{N-1}$. This single-ended LSB switching reduces the required total capacitance by half, compared to the conventional split-MSB capacitor array approach [11]. The only problem it brings is a CM voltage variation at the inputs of the comparator during the LSB switching. However, this CM voltage variation, with amplitude of LSB/2, is insignificant. In addition, unlike the $V_{\text{cm}}$-based SAR ADCs, this architecture does not require an extra dc voltage $V_{\text{cm}}$, and the buffer driving it.

Lastly, a prior work [7] showed that different supplies for the analog and digital parts lower the overall power consumption without hurting the performance of an SAR ADC that operates at 2 kS/s. The dual supply approach is adopted in this ADC which operates at a higher rate, up to 1.1 MS/s.

The switches for connection to $V_{\text{ref}}$ or ground are realised by P-type metal-oxide-semiconductor (PMOS) or N-type metal-oxide-semiconductor (NMOS). The switch configuration is practically an inverter as illustrated in Fig. 3. The inverter is controlled by its corresponding bit ($b_i$) during the binary searching process. Both charging and discharging target capacitor $xC_0$ draw energy from $V_{\text{ref}}$. The capacitors $yC_0$ and $zC_0$ represent the rest of the capacitors in the CDAC that are connected to ground and $V_{\text{ref}}$. Let the parasitic capacitor $C_{bp}$ at the bottom plate be $\lambda C_0$, which is often much smaller than the total capacitance of the CDAC [10]. The energies delivered from $V_{\text{ref}}$ for charging ($E_C$) and discharging ($E_D$) $xC_0$ are derived as

$$E_C = \frac{x \cdot (z + \lambda)}{x + y + z\lambda} C_0 V_{\text{ref}}^2$$

$$E_D = \frac{x \cdot y}{x + y + z\lambda} C_0 V_{\text{ref}}^2$$

For the parasitic capacitance $C_{bp}$ at the bottom plate, it presents a direct loading to the inverter, which should be minimised with careful layout. Note here that the energies dissipated by $C_{bp}$ are not covered in (3) and (4).

Based on (3) and (4), the switching energy for different output codes (different values of $x$, $y$ and $z$) is evaluated as shown in Fig. 4, which ignores the parasitic capacitances. The averaged energy consumption, assuming an even distribution of the output codes, is also shown in Fig. 4.

For the LSB-down scheme, its switching energy is about the same as that of the current best one, namely, the $V_{\text{cm}}$-based.

**Fig. 1** SAR ADC architecture

**Fig. 2** Voltage waveforms at the CDAC outputs in

a Split-MSB with LSB-down scheme

b Conventional BWA scheme

$V_{\text{ip}} = V_{\text{ref}}$ and $V_{\text{in}} = 0$ V are assumed in this example

**Fig. 3** Charging and discharging the CDAC

2.2 CDAC switching energy

The switches for connection to $V_{\text{ref}}$ or ground are realised by P-type metal-oxide-semiconductor (PMOS) or N-type metal-oxide-semiconductor (NMOS). The switch configuration is practically an inverter as illustrated in Fig. 3. The inverter is controlled by its corresponding bit ($b_i$) during the binary searching process. Both charging and discharging target capacitor $xC_0$ draw energy from $V_{\text{ref}}$. The capacitors $yC_0$ and $zC_0$ represent the rest of the capacitors in the CDAC that are connected to ground and $V_{\text{ref}}$. Let the parasitic capacitor $C_{bp}$ at the top plate be $\lambda C_0$, which is often much smaller than the total capacitance of the CDAC [10]. The energies delivered from $V_{\text{ref}}$ for charging ($E_C$) and discharging ($E_D$) $xC_0$ are derived as

$$E_C = \frac{x \cdot (z + \lambda)}{x + y + z\lambda} C_0 V_{\text{ref}}^2$$

$$E_D = \frac{x \cdot y}{x + y + z\lambda} C_0 V_{\text{ref}}^2$$

For the parasitic capacitance $C_{bp}$ at the bottom plate, it presents a direct loading to the inverter, which should be minimised with careful layout. Note here that the energies dissipated by $C_{bp}$ are not covered in (3) and (4).

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For the LSB-down scheme, its switching energy is about the same as that of the current best one, namely, the $V_{\text{cm}}$-based.
approach. The peak switching energy happens at the mid-scale because it invokes the largest charge redistribution. The idea of energy saving is to reduce the capacitance by half for the same unit capacitor, while that behind the \( V_{\text{cm-based}} \) approach is to reduce the step-size of voltage to be switched by 1/2 during the transition with an extra reference voltage \( V_{\text{ref}} \).

A CDAC architectural coefficient \( \beta \) is defined here, which measures the average switching energy of a CDAC normalised to that of the BWA CDAC. The values of \( \beta \) for different CDACs are compared in Table 1.

### 2.3 CDAC linearity

The ADC linearity is mainly affected by the capacitor mismatch in the CDAC. Model the actual value of a capacitor as the sum of its nominal capacitance and an error term \( \delta_i \):

\[
C_i = 2^{N-i}C_0 + \delta_i, \quad \sigma_i^2 = E[\delta_i^2] = 2^{N-i}\sigma_0^2
\]

where the error term \( \delta_i \) is a random variable with a zero mean and a variance of \( \sigma_i^2 \). The \( \sigma_0 \) is the standard deviation of the unit capacitance. It is reasonable to assume that the capacitors in the positive half circuits have the same mismatch properties as those in the negative half. The largest accumulated capacitor mismatch, and thus the worst differential non-linearity (DNL) and integral non-linearity (INL), occurs at \( \delta_d + 1/4\delta_{\text{ref}} \) and \( 3/4\delta_{\text{ref}} \). The standard deviations of the worst DNL and INL (end-point fit) of this SAR ADC, because of capacitor mismatch, are found as

\[
\sigma_{\text{DNL,max}} = \frac{1}{2}2^{N/2}\frac{\sigma_0}{C_0} \text{LSB}
\]

\[
\sigma_{\text{INL,max}} = \frac{\sqrt{2}}{4}2^{N/2}\frac{\sigma_0}{C_0} \text{LSB}
\]

The 10-bit resolution, the theoretical DNL and INL are 0.1 and 0.08 LSB, respectively. From (6) and (7), the theoretical DNL and INL are 0.1 and 0.08 LSB, respectively. Lastly, customised capacitors [17] can be used for smaller area and power.

### 3 Building block circuits

#### 3.1 Passive sample-and-hold (S/H) circuit

The passive S/H circuit in the SAR ADC must be fast enough to meet the settling requirements. For a sampling error less than 1/2 LSB for \( N \)-bit resolution, the \(-3\) dB bandwidth of the S/H circuit must be at least \( 0.69(N+1)T \), where \( T \) is the duration of the available sampling time. In a synchronous SAR ADC, it takes \((N+1)\) clock periods to convert one sample. As a result, the minimum \(-3\) dB bandwidth of the S/H is \( 0.69(N+1)f_{\text{clk}} \), where \( f_{\text{clk}} \) is the clock rate. The sampling time is assumed to occupy one clock period.

In this design, a switch on-resistance less than 690 \( \Omega \) is required for \( N = 10 \), \( C_S \approx 15 \mu F \) and \( f_{\text{clk}} = 500 \text{ KHz} \). To avoid using large size switches, bootstrapped switches [17] are used. Monte Carlo runs under the worst corner (ss, hot and low \( V_{\text{DD}} \)) gives a signal-to-distortion-and-noise ratio (SNDR) with a mean of 66 dB and a standard deviation of 1 dB, which is within the design target.

### 3.2 Dynamic comparator

Fig. 5 shows the dynamic comparator [18] designed for this ADC. A number of measures have been taken. First, NMOS input pairs are used for higher speed and smaller size. Second, a pair of balanced buffers is inserted before set-reset (SR) latch for smaller offset. The offset of comparator hurts the input swing and degrades the signal-to-noise ratio (SNR) although it does not affect the linearity of the ADC [13]. Monte Carlo simulations show that the comparator’s offset voltage is less than 25 mV with a 99.7% confidence level. This amount of offset degrades the SNR by

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**Table 1** Comparison of different CDAC switching schemes

<table>
<thead>
<tr>
<th>Switching procedures</th>
<th>Normalised switching energy (( \beta ))</th>
<th>Normalised total capacitance</th>
<th>Normalised ( \sigma_{\text{DNL}} )</th>
<th>Normalised ( \sigma_{\text{INL}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>BWA</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>split-capacitor</td>
<td>0.63</td>
<td>1</td>
<td>0.71</td>
<td>1</td>
</tr>
<tr>
<td>energy saving</td>
<td>0.44</td>
<td>1</td>
<td>0.5</td>
<td>0.25</td>
</tr>
<tr>
<td>set-to-down</td>
<td>0.19</td>
<td>0.5</td>
<td>0.71</td>
<td>0.35</td>
</tr>
<tr>
<td>( V_{\text{cm-based}} )</td>
<td>0.13</td>
<td>0.5</td>
<td>0.71</td>
<td>0.5</td>
</tr>
<tr>
<td>w/LSB down</td>
<td>0.13</td>
<td>0.5</td>
<td>0.71</td>
<td>0.35</td>
</tr>
</tbody>
</table>

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0.22 dB because of the reduction on the dynamic range. Third, the thermal noise of the comparator is tailored into the level of quantisation noises by setting the total load capacitor (including parasitic) at the comparator output to be larger than 10 fF [7].

3.3 Digital controller
A low-power digital controller is designed using clock gating technique, as shown in Fig. 6. True single-phase flip-flops (TSPF) [19] are used for its fewer transistor numbers and low-power consumption. In each bit-resolving clock cycle, at most two registers alter their outputs. A transmission gate, controlled by proper logics, is thus inserted to modulate the clock to save power. Besides, enabled by low-$V_t$ transistors, 0.5 V supply is used in the digital controller to reduce its dynamic power dissipation. A level shifter [20] is used for interface between the analog (1.0 V) and digital parts (0.5 V). A limitation of the TSPF, like other dynamic

![Fig. 6 Clock-gated shifter register based on TSPF](image)

![Fig. 7 Micrograph of the ADC](image)

![Fig. 8 Measured DNL/INL plot](image)

![Fig. 9 4 k-point FFT for an input frequency near $f_s/2$ and $f_s = 1.1$ MS/s](image)

![Fig. 10 Measured dynamic performance against input frequency at 1.1 MS/s](image)

![Fig. 11 Measured FOM against sampling frequency](image)

**Table 2** Comparison of different switching procedures

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.13 µm 1P6M CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling rate</td>
<td>1.1 MS/s</td>
</tr>
<tr>
<td>Core area (w/I/O buffer)</td>
<td>821 × 665 µm²</td>
</tr>
<tr>
<td>DNL [LSB]</td>
<td>+0.6/−0.7</td>
</tr>
<tr>
<td>INL [LSB]</td>
<td>+1.3/−1.6</td>
</tr>
<tr>
<td>SNDR/SFDR (at $f_m - f_s/2$)</td>
<td>55.2 dB/62.2 dB</td>
</tr>
<tr>
<td>ADC power breakdown at 1.1 MS/s</td>
<td>1.2 1.2 1.0 1.0</td>
</tr>
<tr>
<td>Supply voltage (V) in comparator and level shifter</td>
<td>1.2 1.2 1.0 1.0</td>
</tr>
<tr>
<td>DAC power consumption (µW) in comparator and level shifter</td>
<td>8.4 8.5 5.0 5.0</td>
</tr>
<tr>
<td>ADC FOM</td>
<td>64.7 49.4 65.5 44.1</td>
</tr>
</tbody>
</table>

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memory circuits, it is that must operate above a certain clock rate to avoid losing its internal memory status because of charge leakages.

4 Measurements results

A 10 bit SAR ADC was designed and fabricated in a 0.13 μm CMOS process. A micro-photograph of the die is shown in Fig. 7. The ADC core area is 821 × 665 μm², including the I/O buffers. The capacitor array occupies about 55% of the active chip area because we used the standard MIM capacitors, the size of one of which is 5.24 μm × 5.24 μm or larger.

A differential 5 kHz sinuisoidal input signal with 0 dB FS amplitude was applied to the 1.1 MS/s, 10 bit ADC for the static linearity measurement of ADC [21]. Fig. 8 shows the measured DNL and INL. The peak DNL error is +0.6/−0.7 LSB and the peak INL error is +1.3/−0.7 LSB, which are larger than the theoretical values from (6) and (7). The deviation is attributed to wide separation between some capacitors and systematic mismatch errors, including routing mismatch, second-order oxide thickness variation and parasitic effects at the internal nodes of LSB capacitors.

Table 3 SAR ADC comparison with different switching procedures

<table>
<thead>
<tr>
<th>Switching procedures</th>
<th>Process, nm</th>
<th>Supplies, V</th>
<th>Unit cap., fF</th>
<th>fREF, MS/s</th>
<th>ENOB, bit</th>
<th>Power, µW</th>
<th>FOM, fJ/conv.-step</th>
<th>FOMa, fJ/conv.-step-fF</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1] Hong ‘07</td>
<td>single-ended BWA</td>
<td>180</td>
<td>0.9</td>
<td>24</td>
<td>4</td>
<td>0.4</td>
<td>7.31</td>
<td>6.15</td>
</tr>
<tr>
<td>[12] Chang ‘07</td>
<td>energy saving</td>
<td>180</td>
<td>1.0</td>
<td>20</td>
<td>0.5</td>
<td>75</td>
<td>7.75</td>
<td>86</td>
</tr>
<tr>
<td>[22] Craninckx ‘07</td>
<td>charge sharing</td>
<td>90</td>
<td>1.0</td>
<td>64</td>
<td>20</td>
<td>7.8</td>
<td>290</td>
<td>65.1</td>
</tr>
<tr>
<td>[6] Elzakker ‘08</td>
<td>adiabatic charging</td>
<td>65</td>
<td>1.0</td>
<td>—</td>
<td>0.6</td>
<td>1</td>
<td>8.75</td>
<td>1.9</td>
</tr>
<tr>
<td>[13] Liu ‘10</td>
<td>set-to-down</td>
<td>130</td>
<td>1.2</td>
<td>4.5</td>
<td>50</td>
<td>9.18</td>
<td>826</td>
<td>29</td>
</tr>
<tr>
<td>[14] Zhu ‘10</td>
<td>1.2</td>
<td>50</td>
<td>100</td>
<td>9.1</td>
<td>3000</td>
<td>55</td>
<td>1.1</td>
<td></td>
</tr>
<tr>
<td>[16] Tripathi ‘13</td>
<td>split-MSB w/LSB down</td>
<td>65</td>
<td>1.2</td>
<td>0.75</td>
<td>450</td>
<td>7.56</td>
<td>6480</td>
<td>76</td>
</tr>
<tr>
<td>[17] Harpe ‘11</td>
<td>custom capacitor</td>
<td>90</td>
<td>1.0</td>
<td>0.932</td>
<td>10.24</td>
<td>7.77</td>
<td>26.3</td>
<td>12</td>
</tr>
<tr>
<td>[2] Xu ‘12</td>
<td>cap. with calibration</td>
<td>180</td>
<td>3.3/1.8</td>
<td>20</td>
<td>0.768</td>
<td>9.8</td>
<td>58</td>
<td>74</td>
</tr>
<tr>
<td>[23] Liu ‘10</td>
<td>windowed switching</td>
<td>180</td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>9.83</td>
<td>98</td>
<td>11</td>
</tr>
<tr>
<td>[24] Liu ‘13</td>
<td>charge average</td>
<td>90</td>
<td>0.4</td>
<td>5</td>
<td>0.5</td>
<td>8.72</td>
<td>0.5</td>
<td>2.37</td>
</tr>
<tr>
<td>[25] Harpe ‘13</td>
<td>custom capacitor</td>
<td>65</td>
<td>0.6</td>
<td>0.25</td>
<td>0.04</td>
<td>9.4</td>
<td>0.072</td>
<td>2.7</td>
</tr>
</tbody>
</table>

This work split-MSB w/LSB down | 130 | 1.0/0.5 | 29.8 | 1.1 | 8.9 | 23.2 | 44.1 | 1.5 |

5 Conclusions

An SAR ADC with an energy-efficient CDAC, namely, the split-MSB with LSB down, has been presented. Theoretically, given the same unit capacitor, this switching scheme achieves the best energy efficiency under the same DNL and INL performance. With an optimised clock-gated digital controller using TSPF and a lower digital supply, the 0.13 μm CMOS ADC achieves 8.9-ENOB at 1.1 MS/s, and an FOM of 44.1 fJ/conversion-step. Table 3 compares the measured result to state-of-the art SAR ADCs with different switching schemes. Normalising the FOM to the unit capacitance, denoted as FOMa, representing the architectural FOM, this switching scheme is among the most energy efficient.

6 Acknowledgment

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7 References


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