A Digital-Control Sensorless Current-Mode Boost Converter with Non-Zero Error Bin Compensation and Seamless Mode Transition

Yanqi Zheng, Marco Ho, Ka Nang Leung, Jianping Guo and Biao Chen
Email: {yqzheng, mho, knleung}@ee.cuhk.edu.hk  guojp3@mail.sysu.edu.cn  chenb56@mail2.sysu.edu.cn
*Department of Electronic Engineering, The Chinese University of Hong Kong, Hong Kong SAR, China
†School of Physics and Engineering, Sun Yat-sen University, Guangzhou, China
‡SYSU-CMU Shunde International Joint Research Institute, Foshan, China

Abstract—A digital-control sensorless current-mode boost dc-dc converter is presented in this paper. By using the proposed sensorless current-mode control, the requirement for implementation of current sensor for conventional current-mode dc-dc converter is relaxed. Moreover, the converter can seamlessly switch between CCM and DCM operation as in conventional current-mode control. With this method, the non-limited-cycle for digital-control current-mode converter is realized. Lower resolution of DPWM can be used to avoid the appearance of limited cycle, regardless of loading condition.

Keywords—boost converter, current program mode, dc-dc converter, digital control, limited cycle oscillation.

I. INTRODUCTION

Current program mode (CPM) dc-dc converter [1-7] is a popular solution for the control of dc-dc converter. Comparing to its counterpart voltage program mode (VPM), CPM reduces the order of output filter of the power stage by adding an inductor current feedback loop. As a result, usually, a second-order filter which contains a single zero is sufficiency to compensate the feedback loop. Moreover, the characteristic of CPM dc-dc converter is similar and have the same order when it operates in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Therefore, the transition between these two modes which is dependent on loading condition is smoother and easier than that of VPM. However, current sensor is the major cost which increases the design challenge. On the other hand, digital control is more and more preferred in power management IC design because of its flexibility, process independent and programmable. However, because of the quantization, a phenomenon of limited cycle will appear if the resolution of the digital pulse width modulator (DPWM) is not high enough.

In this paper, a sensorless current program mode dc-dc converter is presented. Different from the convention current mode control method, the proposed converter does not have a constraint in sensor accuracy. The challenge of accurately predicting the ESR of inductor, which defines the dc gain of the sensor, is no longer necessary. Moreover, by combining the proposed inductor-current constructor and the current-mode duty-cycle generator, the high sampling rate of inductor-current sensor is no longer necessary, which highly reduces the design complexity and power consumption. Finally, the resolution requirement for the DPWM of the proposed design is released when compared to the conventional digital-control current-mode PWM generator.

This paper is organized as follows. First, a short discussion and analysis of the prior technique of current sensor and their limitation will be given. Then the proposed inductor-current reconstruction and its application to sensorless current-mode dc-dc converter will be analysed in detail. The requirement for current-mode dc-dc converter and its relationship between CPM and VPM will then be derived. A digital controller with the proposed sensorless current mode dc-dc converter will be presented. Finally, simulation will be given to verify the proposed idea and conclusion will be given.

II. DIGITAL-CONTROL CURRENT-MODE DC-DC CONVERTER

A digital-control current-mode [1-3] dc-dc boost converter is shown in Fig. 1. It is combined with a power stage, voltage ADC, inductor-current sensor, inductor-current ADC, PI controller, DPWM and auxiliary control logic and gate driver.

Fig. 1. Circuit diagram of digital-control current-mode boost converter with inductor sensor and quantization.
The general design rule-of-thumb of non-limited-cycle condition is that shown in (1), which means that the resolution of DPWM should be increased corresponding to the increase of resolution of the voltage ADC. However, this is not true for the digital-control current-mode converter. In the circuit diagram of Fig. 1, the resolution of DPWM can be much lower than the corresponding result shown in (1), since output duty cycle is controlled by the inductor-current feedback loop shown in Fig. 2. As a result, this can be treated as an intrinsic sigma-delta DPWM and the average of duty cycle, \( d \), is equivalent of making the sensing inductor current \( i_{sen} \) equal to the current control signal \( i_c \). However, this does not mean that the requirement for resolution of DAC in current mode is lower than voltage mode. Consequently, according to the transfer function of the converter, the non-limited-cycle condition for this topology is shown in (2) and (3).

\[ q_{dyn} < \frac{1}{V_v} \]  \hspace{1cm} (1)
\[ \Delta V_v = \frac{V_v}{I_o} \Delta i_o \]  \hspace{1cm} (2)
\[ q_{ic} < \frac{I_o}{V_v} \]  \hspace{1cm} (3)

It can be seen that, the resolution requirement for \( i_c \) and \( i_{sen} \) are now highly dependent on the loading condition, which is not preferred and sometimes difficult to be fulfilled. Moreover, due to the design challenges for the current sensor and corresponding ADC, the operation frequency of this type of digital-control current-mode converter cannot be high.

A reported solution for eliminating current ADC is to use the hybrid-control current-mode [4], as shown in Fig. 3. It shows that the current control signal \( i_c \) is converted to analog signal with the charge-pump-based DAC and then compared with the sensed inductor current. As a result, the inductor current control is eliminated and the operation speed can be increased. However, with this solution, the resolution requirement for the DAC still depends on (3).

Moreover, as opposed to the voltage-mode control method, in the PI controller for the digital-control current-mode dc-dc converter shown in Fig. 2, the total resolution of the controller is fully dependent on the integration factor \( k_p \), while \( k_i \) only defines the overflow input voltage of \( v_c \). As a result, the dynamic parameter of the controller is in strong relationship with the selection of resolution in the digital compensator design, which is stronger than the input and output quantization relationship. For example, if the controller requires a high resolution for the ultra-light-load condition, the integration factor has to be smaller to provide the LSB signal. This results in a low-frequency zero in the PI controller and makes the small-signal settling time very long due to the non-cancelled pole-zero doublets.

![Fig. 2. PI controller for digital-control current-mode dc-dc converter shown in Fig. 1.](image1)

![Fig. 3. Hybrid-control current-mode dc-dc converter with charge-pump-based DAC.](image2)

### III. PROPOSED SENSORLESS CURRENT PROGRAM MODE CONTROL METHOD

#### A. Non-zero error bin compensation (NZEBC) in digital-control dc-dc converter

To solve these problems, a new PI controller with non-zero error bin compensation is shown in Fig. 4.

\[ s_{zn} = q_{vn}/2 \]

![Fig. 4. PI controller with non-zero error bin compensation for current mode dc-dc converter.](image3)
be neglected, which means its magnitude is much smaller than $q_{ve}$. The steady-state magnitude of this intrinsic limited cycle can be derived by the loop transfer function of the dc-dc converter shown in Fig. 6 and the describing function of the ADC shown in Fig. 5(b). In Fig. 6, $z_0$ is the zero generated by the PI controller, $p_0$ is pole generated by the power stage of current-mode control dc-dc converter. $\omega_0$ is the target bandwidth, $\omega_s$ is the operation frequency and $\omega_i$ is the intrinsic limited cycle frequency. It should be noted that the phase of the loop transfer function will degrade towards -180° because the dc-dc converter is a sampling system. The describing function of voltage quantization zero error bin and non-zero error bin are shown in Fig. 5(b). The parameter $a$ represents the normalized input amplitude which equal to the magnitude of input of voltage ADC over quantization level $q_{ve}$ and $G(a)$ represents the gain of the ADC. Since the gain of the ADC in non-zero error bin quantization can be treated as infinite, oscillation will certainly appear as indicated above. However, due to the nonlinearity of the quantizer, the gain is signal-dependent and will be decreased when the magnitude of input signal to ADC increases as indicated with blue line in Fig. 5(b). From (6), it shows that magnitude of intrinsic limited cycle can be reduced with a larger output capacitor, since $k_p$ is inversely proportional to output capacitor. Moreover, the voltage accuracy is improved because of eliminating the open loop operation with conventional quantization with zero error bin. All of these cannot be achieved by other technique for reducing resolution of DPWM such as dithering and sigma-delta DAC [8].

**B. Architecture of current observer of the proposed sensorless digital-control current-mode boost converter**

![Fig. 7. SFG of the conventional sensorless current controller.](image)

As referred above, with the proposed non-zero error bin compensation, the requirement for the resolution of charge-pump-based DAC is now largely reduced. However, because of the analog current sensor is still required in this hybrid-control current-mode converter, the advantage of fully digital-control implementation is limited. For example, the current sensor normally introduces large noise because of the ringings of $V_c, V_g$ and ground of the power stage. This will increase the possibility of fault trigger of the current comparator which is used to generate the continuous duty cycle. As a result, a conventional solution is to insert a minimum-on-time circuitry or an anti-spiking filter to the current sensor. All of these solutions will limit the dynamic range of the duty cycle generator or affect the maximum bandwidth or operation frequency of the converter. Consequently, the development of digital-control sensorless current mode dc-dc converter is preferred. Previous design has been presented in [5-7], and it requires a current observer which can be simply explained as an inductor current reconstruction. The signal-flow graph (SFG) of this design is shown in Fig. 7. The gain factors $k_{i3}, k_{i5}, k_{i7}$ stand for the gain from duty cycle command, input voltage and output voltage to inductor current, respectively. It can be shown that if the integrator of the inductor current observer is fully matched to the effect of inductor current, the reported implementation is actually preferred since the quantization of...
$V_g, V_o$ and duty cycle are easier to be achieved. However, since the parasitics and variation of the power device (such as the ESR of the inductor) will make the exact inductor current model violate the inductor current observer in steady state, and cause $i_{mfb}$ to continue to increase or decrease until it overflows. Although a proper overflow protection in digital controller can still make converter continue to function, a steady-state voltage error is introduced since the integrated effect of the PI controller is cancelled by the integrator of the current observer.

![Fig. 8. SFG of the proposed sensorless current controller without dc error.](image)

![Fig. 9. SFG of the proposed sensorless current controller with anti-windup.](image)

To solve this, two sensorless current controllers are proposed and shown in Figs. 8 and 9. In Fig. 8, it shows that an internal feedback is constructed with $k_{p2}$ to compensate the steady-state error by the exact current sensor and current observer. As a result, the dc gain, which was originally infinite, becomes bounded to a finite value defined by $k_{p2}$. The magnitude of $k_{p2}$ affects the zero location of the transfer function from $i_c$ to $d$, which now can be treated as a PD controller. Moreover, if the observer output is required to track with $i_{mref}$ without dc error, an integration part can be inserted with the factor $k_{i2}$ as shown in Fig. 9. Provided that $i_{mref}$ is constant, the proposed controller in Fig. 9 is similar to a voltage-control PID controller if the input voltage feedforward path is ignored. Moreover, this can guarantee no integrator windup even the current observer is much diverted from the exact inductor current in Fig. 8. However, it should be noted that because of the integrator effect, $d$ can drift away from the steady-state value as long as $i_c$ is constant with different $d_{tune}$. As a result, it is necessary to employ the non-zero error bin compensation to make the magnitude of $d$ to be regulated by the closed voltage loop. On the other hand, it shows that if an actual inductor current is needed, a slow but accurate inductor current sensor and ADC can be used and fed into $i_{mref}$.

### C. Seamless transition between DCM and CCM for the proposed converter

As referred above, an advantage of current-mode control of dc-dc converter against voltage-mode control is the seamless transition between CCM and DCM. This is due to the fact that the compensation architecture for voltage mode is PID in CCM and PD in DCM, while it is PI for both cases in current mode. However, in sensorless current-mode control dc-dc converter, because it is a virtual inductor current created by the observer instead of a true inductor current, it is no more than a voltage controller without the input voltage feedforward. As a result, a proper design should be done to solve the problem during mode transition. In this design, the seamless auto mode transition (AMT) technique is proposed as shown in Fig. 10. It is shown that when the signal $dcm\_en$ turn to 1, which indicates the inductor current fall down to zero during the normal operation, the current feedback loop should be broken so that the equivalent PID controller of the sensorless current-mode for CCM operation transfers to a PI controller for DCM operation mode. As $i_{mfb}$ will be regulated by $i_{mref}$, its perturbation to the main control loop should be eliminated. This is accomplished by the differentiator as shown in the dark area in Fig. 10. As a result, during mode transition, there is no internal state variable being saturate or windup and they can immediately recover when the converter transfer from DCM to CCM.

![Fig. 10. SFG of the proposed sensorless current controller with seamless transition between DCM and CCM.](image)
will be verified by simulation results. The top-level circuit diagram of the proposed design is shown in Fig. 11.

\[
\frac{1}{2L}V_o^2 DT, \frac{1}{V_o - V_g} DT, \frac{1}{T_s} = \frac{1}{R} \quad V_o = \frac{V_o}{R} \tag{7}
\]

\[
\Delta V_o = \frac{2V_o}{D} \Delta d \tag{8}
\]

\[
q_{PWM} < q_o \quad \frac{D}{2V_o} = q_o \quad 1 \quad \frac{1}{2V_o} \sqrt{\frac{2L(I_o - V_g)}{V_g - V_g}} \quad \tag{9}
\]

Fig. 11. Proposed sensorless digital-control current-mode boost converter.

IV. SIMULATION RESULTS

In order to verify the proposed method, a digital-control sensorless current-mode boost converter is modelled in Simulink based on Fig. 11. The simulation parameters are as follows: \(V_G = 3V\), \(V_o = 5V\), \(L_1 = 2.2\mu H\), \(R_{ESR,L1} = 150m\Omega\), \(C_1 = 10\mu F\), \(R_{ESR,C1} = 20m\Omega\), \(f_s = 1MHz\). For comparison, a converter with digital-control voltage-mode boost converter has also been modelled, and their simulation results are shown in Figs. 12–16. In Fig. 12, it shows that limited cycle oscillation appears in conventional converter when \(N_{DPWM}\) falls down to 9-bit. On contrast, Fig. 13 shows that a lower resolution of DPWM can be used to implement the digital-control current-mode controller in the proposed method without triggering the LSB of the voltage quantizer when the resolution of DPWM falls down to 7-bit. Although there is intrinsic limited cycle and its magnitude is related to \(N_{DPWM}\) as predicted in (6) and shown in Fig. 13, their amplitudes are neglected when compared to the case shown in Fig. 12(b). Moreover, benefited from the non-zero error bin compensation, the output voltage accuracy will not degrade even though a low resolution ADC is used, which is demonstrated in Fig. 14(a). Fig. 14(b) also verified that although with a high resolution DPWM, the output voltage accuracy is still poor with the conventional zero-error bin quantization. Fig. 15 shows that the seamless transition between DCM and CCM with the proposed auto mode transition (AMT) method. Finally, Fig. 16(a) demonstrates that limited cycle oscillation appears when the converter enters DCM even it operates in voltage mode, which verifies (9). On the other hand, the proposed method generates no limited cycle in DCM as shown in Fig. 16(b).
V. CONCLUSIONS

A novel topology of digital-control sensorless current-mode boost converter is proposed. With the proposed non-zero error bin compensation and sensorless current-mode control algorithm, the resolution requirement for DPWM and the internal DSP is largely reduced. Moreover, the undesirable relationship between compensation parameter and resolution requirement is also eliminated. Finally, the voltage regulation can be guaranteed even with a low-resolution voltage ADC. The increasing resolution requirement of DPWM in DCM mode is also solved. Simulation results have been shown to verify the proposed concept.

REFERENCES


