A Two-Stage Large-Capacitive-Load Amplifier With Multiple Cross-Coupled Small-Gain Stages

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Abstract—A two-stage large-capacitive-load amplifier with multiple cross-coupled small-gain stages is proposed in this paper. The cross-coupled structure of the small-gain stages augments the large-signal responses, providing significant improvement in the effective output-stage transconductance and, hence, the gain–bandwidth product (GBW). Implemented in a standard 0.13-μm CMOS technology and powered by a 0.7 V supply with a current consumption of 20 μA, the proposed amplifier achieves the GBW of 1.17 MHz and the phase margin of 74.8° while driving a capacitive load of 9.5 nF. The average slew rate is 0.3679 V/μs. The on-chip compensation capacitor is only 1.62 pF. The active chip area is 0.0056 mm².

Index Terms—Miller compensation, slew rate (SR), small-gain stages, two-stage amplifier.

I. INTRODUCTION

Frequency compensation of multistage amplifiers has been extensively researched for more than two decades [1]–[18]. The main focuses of this paper are to extend the gain–bandwidth product (GBW) with sufficient phase margin (PM) using very small compensation capacitors. The achievable GBW of a three-stage amplifier driving large capacitive load compensated by appropriate topology can be much wider than a single-stage or a two-stage amplifier [8]–[18]. Meanwhile, the added high-gain stages generate extra high-impedance nodes, and hence, more compensation capacitors are needed. The use of complicated compensation structures would undoubtedly degrade the robustness and the reliability of the amplifier. The required stability criteria obtained by tedious calculations keep circuit designers away from using the developed compensation topologies. In fact, the two-stage simple Miller-compensated (SMC) amplifier structure is a much preferred choice, since this circuit concept is well-known among the analog circuit designers, and also, the two-stage structure has been widely used in many IC systems for a long time. The only drawback is that the GBW is not sufficiently wide in the low-power and large-capacitive-load condition [8]–[18].

There are many compensation topologies proposed in the past two decades. The common goal is to solve the bandwidth reduction problem due to Miller compensation for two-stage and three-stage amplifiers [1]–[18]. Multipath nested Miller compensation [1], [6], hybrid nested Miller compensation [2], and nested $G_m - C$ compensation [7] are based on the signal bypass through the Miller compensators at high frequencies to extend bandwidth. Meanwhile, the damping-factor-control frequency compensation solves the problem of self-capacitive loading generated by the inner-loop compensation capacitor [8]. AC-boosting compensation makes use of a signal feedforward capacitor to bypass signal voltage to the gate of the output transistor in order to enhance the high-frequency effective transconductance of the output stage and, hence, the overall bandwidth of an amplifier [11]. The outcomes are significant in terms of bandwidth enhancement, but the main drawback is that on-chip capacitors are always required. Thereafter, in the last decade, impedance adapting compensation [13], cross-feedback cascode compensation [14], and compensation schemes with current buffer and pole-zero cancellation [15], [16] were proposed. The pole-zero cancellation at the second stage achieves phase compensation, such that the second stage becomes a virtually phase-shift-free stage as a pure gain stage to enhance the transconductance of the output stage for bandwidth extension. This idea is effective, as proved by experimental results. However, the additional on-chip resistor or active circuit to implement a zero for pole-zero cancellation is obviously a disadvantage. As a matter of fact, pole-zero doublets may increase settling time. Methods to increase the effective transconductance of the output stage for two-stage Miller-compensation amplifiers have been proposed [17], [18]. However, there is still a lot of room to achieve further enhancement. Recently, more works focusing on non-Miller-compensated amplifiers have been reported [19]–[21].

In this paper, a two-stage SMC amplifier with multiple cross-coupled small-gain stages is proposed. The proposed structure is able to significantly increase the effective
transconductance of the second gain stage, such that the
GBW of the amplifier can be substantially extended.
Furthermore, the proposed cross-coupled structure of
the small-gain stages increases the transient current, so that
the slew rate (SR) of the proposed amplifier is also improved.

This paper is organized as follows. Section II presents
a review of the conventional two-stage SMC amplifier
in order to draw attention to its limitations in both the small-
signal and large-signal domains. Section III describes
the concept of using small-gain stages to the two-stage SMC
amplifier and the development of the proposed circuit struc-
ture. Section IV introduces the proposed amplifier structure
in more detail, whereby its stability, small-signal, and large-
signal performances will all be discussed. Section V reports
the experimental results of the proposed amplifier. Finally, the
conclusion of this paper is given in Section VI.

II. TWO-STAGE SIMPLE MILLER-COMPENSATED
AMPLIFIER

The conventional two-stage SMC amplifier is first reviewed
in this section. Both small-signal and large-signal responses
will be scrutinized.

Fig. 1 shows the structure of a two-stage SMC amplifier.
The input and output signal voltages are denoted by \( v_{\text{in}} \)
and \( v_0 \), respectively. The transconductances and the output resistances
of the first and the second gain stages are \( G_{m1} \) and \( G_{m2} \),
as well as \( R_1 \) and \( R_2 \), respectively. The load and compensation capacitors
are \( C_O \) and \( C_m \), respectively. It is noted that
\( C_1 \) is the parasitic capacitor at the output of the first gain stage.

The transfer function of the structure in Fig. 1 is given
by [10]

\[
\frac{v_0(s)}{v_{\text{in}}(s)} = \frac{G_{m1}G_{m2}R_1R_2\left(1 - s \frac{C_m}{G_{m2}}\right)}{(1 + sC_mG_{m2}R_1R_2)(1 + s \frac{C_O}{G_{m2}})}.
\] (1)

From (1), the low-frequency gain is \( G_{m1}G_{m2}R_1R_2 \),
while the dominant pole \( (p_1) \), the nondominant pole \( (p_2) \),
and a right-half-plane (RHP) zero \( (z_{\text{RHP}}) \) are given by [10]

\[
p_1 = \frac{1}{C_mG_{m2}R_1R_2} \quad \quad p_2 = \frac{C_m}{G_{m2}} \quad \quad z_{\text{RHP}} = -\frac{G_{m2}}{C_m}.
\] (2) (3) (4)

To achieve a PM of about 60°, the GBW is designed to be
half of \( p_2 \) (i.e., \( G_{m1}G_{m2}R_1R_2 \times p_1 = p_2/2 \)) to yield [10]

\[
\text{GBW} = \frac{G_{m2}}{2C_O}
\] (5)

and the required compensation capacitor is [10]

\[
C_m = 2 \left( \frac{G_{m1}}{G_{m2}} \right) C_O.
\] (6)

Undoubtedly, \( z_{\text{RHP}} \) reduces the PM, so that it is less than 60°.
From (5) and (6), it is clear that a larger value of \( G_{m2} \) gives
a wider GBW and a smaller value of \( C_m \). With a larger value
of \( G_{m2} \), \( z_{\text{RHP}} \) is located at higher frequency, and so the PM
can be increased.

In order to study the slewing behavior, the implementation
of a typical two-stage SMC amplifier is shown in Fig. 2. The
unit size of the pMOSFETs \([\text{i.e., } (W/L)_{\text{unit}}]\) and nMOSFETs
\([\text{i.e., } (W/L)_{\text{IN}}]\) is indicated above or below the supply lines,
\( V_{DD} \) and \( V_{SS} \), respectively, and the size ratios are denoted by
1, 2, and \( m \) in Fig. 2. \( M_1 \)–\( M_4 \) form the first gain stage, and
\( M_5 \)–\( M_6 \) form the second stage. Results of the low-frequency
gain, nondominant pole, and GBW of this amplifier, based on
(3) and (5), as well as the current consumption are tabulated in Table I.

When a rising step voltage is applied to node \( v_{\text{IN}+}, \)
\( M_2 \) has much more \( v_{GS} \) than \( M_1 \) (momentarily), and thus,
\( M_1 \) is switched OFF. Both \( M_3 \) and \( M_4 \) are in cutoff region.
Node voltage \( v_{U0} \) (i.e., the gate voltage of \( M_5 \)) has no pull-up path and is, therefore, pulled low. Since \( v_{U0} = v_{\text{IN}+} - v_{\text{DS}2} + v_{\text{DS}5} \),
both \( v_{\text{DS}5} \) and \( v_{\text{DS}5} \) depend on \( v_{\text{IN}} \). The positive SR, \( SR^+ \),
is, hence, given by \( (i_{\text{DS}5} - mIB)/C_O \). Similarly, when a falling step voltage is applied to node \( v_{\text{IN}+}, \)
\( M_2 \) is switched OFF, and \( v_{U0} \) is \( \sim V_{DD} \), causing \( M_5 \) to shut down. As a result, the
negative SR, \( SR^- \), is \( mIB/C_O \). Both \( SR^+ \) and \( SR^- \) of this
SMC amplifier implementation are included in Table I.

III. PROPOSED TWO-STAGE MILLER-COMPENSATED
AMPLIFIER WITH MULTIPLE SMALL-GAIN STAGES

Section II reiterates a well-known and important fact that
the GBW of a two-stage SMC amplifier can only be increased
by a larger value of \( G_{m2} \). The benefits are that a smaller value
Table I

Performance Summary of the Studied and the Proposed Structures

<table>
<thead>
<tr>
<th>Amplifier</th>
<th>Gain</th>
<th>$p_1$</th>
<th>GBW</th>
<th>PM</th>
<th>SR$^*$</th>
<th>SR$^*$</th>
<th>$I_{BB}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig. 2</td>
<td>$g_m\beta (r_1/r_2) (s_1/s_2) a/d$</td>
<td>$g_m/C_0$</td>
<td>$g_m/C_0$</td>
<td>$&lt;60^\circ$</td>
<td>$m/(3+1)I_h$</td>
<td>$m/(3+1)I_h$</td>
<td>$m/(3+1)I_h$</td>
</tr>
<tr>
<td>Fig. 5</td>
<td>$k^2 g_m\beta (r_1/r_2) (s_1/s_2) a/d$</td>
<td>$k^2 g_m/C_0$</td>
<td>$k^2 g_m/C_0$</td>
<td>$&gt;60^\circ$</td>
<td>$m/(k+1)I_h$</td>
<td>$m/(k+1)I_h$</td>
<td>$m/(k+1)I_h$</td>
</tr>
<tr>
<td>Fig. 7</td>
<td>$k^2 g_m\beta (r_1/r_2) (s_1/s_2) a/d$</td>
<td>$k^2 g_m/C_0$</td>
<td>$k^2 g_m/C_0$</td>
<td>$&gt;60^\circ$</td>
<td>$m/(k+1)I_h$</td>
<td>$m/(k+1)I_h$</td>
<td>$m/(k+1)I_h$</td>
</tr>
<tr>
<td>Fig. 10</td>
<td>$k^2 g_m\beta (r_1/r_2) (s_1/s_2) a/d$</td>
<td>$m/(k+1)I_h$</td>
<td>$m/(k+1)I_h$</td>
<td>$&gt;60^\circ$</td>
<td>$m/(k+1)I_h$</td>
<td>$m/(k+1)I_h$</td>
<td>$m/(k+1)I_h$</td>
</tr>
<tr>
<td>Fig. 13</td>
<td>$k^2 g_m\beta (r_1/r_2) (s_1/s_2) a/d$</td>
<td>$m/(k+1)I_h$</td>
<td>$m/(k+1)I_h$</td>
<td>$&gt;60^\circ$</td>
<td>$m/(k+1)I_h$</td>
<td>$m/(k+1)I_h$</td>
<td>$m/(k+1)I_h$</td>
</tr>
</tbody>
</table>

Note: The values of $I_{BB}, g_m, g_{in}, r_1, r_2, r_3, r_4$ and $R$ in the above expressions are the same, where $g_{in} = \sqrt{2I_B \mu C_{ox} (W/L)^p}, g_m = \sqrt{2I_B \mu C_{ox} (W/L)^p}$, $g_{in} = \sqrt{2I_B \mu C_{ox} (W/L)^p}, g_m = \sqrt{2I_B \mu C_{ox} (W/L)^p}$.

Fig. 3. Modified structure of the two-stage SMC amplifier with enhanced $G_{m2}$ using wide-bandwidth scalar ($k_m$).

of $C_m$ is needed, and the RHP zero has less effect on the PM. However, more bias current to $M_5$ seems to be unavoidable in order to increase $G_{m2}$, and more power consumption is generally needed.

In order to enhance the effective value of $G_{m2}$, Fig. 3 shows a modified SMC structure with an enhanced $G_{m2}$ for the second gain stage using a wide-bandwidth scalar, $k_m$. The signal voltage generated by the first stage is further scaled by $k_m$ and then applied to the second stage. The effective transconductance of the second gain stage becomes $k_m G_{m2}$.

The bandwidth of the scalar block must be wider than the overall GBW of the amplifier to ensure negligible effect on the phase angle of the propagating signal.

Based on (1), all $G_{m2}$ terms are modified to $k_m G_{m2}$ to give

$$v_o(s) = \frac{G_m k_m G_{m2} R_1 R_2}{(1 + s C_m k_m G_{m2} R_1 R_2)} (1 + s C_m G_{m2}) \left(1 - \frac{s C_m G_{m2}}{1 + s C_m G_{m2}} \right).$$

The modified low-frequency gain is $k_m G_{m2} R_1 R_2$, while the new $p_1$, $p_2$, and $s_{RHP}$ are changed to

$$p_1 = \frac{1}{C_m k_m G_{m2} R_1 R_2},$$
$$p_2 = \frac{k_m G_{m2}}{C_m},$$
$$s_{RHP} = \frac{-k_m G_{m2}}{C_m}.$$

The new GBW for a PM of $60^\circ$ is given by

$$\text{GBW} = \frac{k_m G_{m2}}{2C_m}$$

The modified low-frequency gain is $k_m G_{m2} R_1 R_2$, while the new $p_1$, $p_2$, and $s_{RHP}$ are changed to $p_1 = k', p_2 = k$, and $s_{RHP} = k$, respectively.

Using the concept of multiple small-gain stages reported in [22], a wide-bandwidth scalar block with two cascaded small-gain stages (Stage 1 of $M_{11}$ and $M_{12}$, and Stage 2 of $M_{21}$ and $M_{22}$) with a second gain stage (i.e., $M_5$) is implemented and shown in Fig. 4. Referring to Fig. 2, the dc bias at the gate of $M_5$ is $V_{DD}$, where $V_{DD} = V_{DD} - V_B$ in Fig. 4. With the introduction of the small-gain stages, the same bias condition of $M_5$ can still be retained to provide an identical value of $g_m$. From Fig. 4, it is clear that with a bias current of $(k+1)I_B$, where $k$ is the size ratio of $M_{11}$ to $M_{12}$ (the same applies to $M_{21}$ and $M_{22}$), the $V_{DS}$ drops of $M_{11}$, $M_{12}$, $M_{21}$, $M_{22}$, and $M_5$ are exactly the same. It implies that the dc gate voltage of $M_5$ is still $V_{DD}$ after passing through two small-gain stages.

The signal voltage at the gate of $M_{11}$ is increased from $v_{G1}$ to $-k v_S$ due to the first small-gain stage and then to $k^2 v_S$ after the second stage. As a result, the small-signal output current of $M_5$ becomes $k^2 g_m V_S$, which implies that the effective transconductance of the second gain stage (i.e., the signal points between $v_{G1}$ and $v_S$) is increased by $k^2$ times, a quadratic relationship of $k$. Therefore, the value of $k_m$ in (7)–(12) is $k^2$, where $k > 1$ is set for achieving...
small-signal improvement. It is noted that the increase of bias current due to the small-gain stages is simply $2(k+1)I_B$, which is a linear relationship of $k$.

Fig. 5 shows the full schematic of the SMC amplifier with two cascade small-gain stages. The modification is easily done through inserting the cascade small-gain stages between the output of the first gain stage (i.e., the drains of $M_2$ and $M_3$) and the input of the second gain stage (i.e., the gate of $M_5$). The current consumption ($I_{DD}$) of this amplifier is $(m+2k+5)I_B$. $V_{B1}$ is the dc bias voltage generated by $I_B$ and $M_{B2}$. The low-frequency gain is $k^2g_{m3}g_{m5}(r_{o2}/r_{o4})(r_{o5}/r_{o6})$. As $p_2 = k^2g_{m5}/C_O$, $GBW = k^2g_{m5}/(2C_O)$ for a PM of about 60°. The required $C_m$ is reduced by $k^2$ times to allow $f_{RHP}$ to be located at an even higher frequency, according to (10). The small-signal performance is included in Table I.

For large-signal performance, the step responses of the SMC amplifier with two cascade small-gain stages are provided in Fig. 6(a) and (b).

Fig. 6(a) shows that when a rising step is applied to $v_{IN+}$, $M_2$ obtains more $v_{GS}$ momentarily. The tail current equals to the drain current of $M_2$, and it is also the current to discharge $C_m$. $M_1$, $M_3$, and $M_4$ are switched off. Node voltage $v_{UD0}$ is pulled to $v_{IN+} - v_{GS2} + v_{DS2}$. In fact, $M_{U11}$ and $M_{U13}$ form a current comparator [23], and thus, $v_{U1}$ is pulled high. As a result, both drain currents of $M_{U11}$ and $M_{U13}$ are a little larger than $(k+1)I_B$ due to the smaller $V_{SD}$ of $M_{U11}$ and larger $V_{GS}$ of $M_{U13}$. $M_{U12}$ and $M_{U21}$ are then switched off. The current of $M_{U22}$ equals to that of $M_{U23}$. With the current-mirror ratio of $M_{U22}$ to $M_5$ (i.e., $m$), the transient current from $M_5$ is $m(k+1)I_B$. By subtracting the static bias current of $M_5$, the transient output current to charge $C_O$ is $m(k+1)I_B - mI_B = mkI_B$. Thus, $SR^+ = mkI_B/C_O$.

Similarly, referring to Fig. 6(b), when a falling step is applied to $v_{IN+}$, $M_2$ is switched off momentarily. The resultant effect is that $M_5$ is switched off, and the discharging current of $C_O$ contributed by $M_6$ is $mI_B$. Thus, $SR^- = mI_B/C_O$, which is independent of $k$.

Although this circuit structure enables faster small-signal response, the large-signal response is not outstanding due to the Class-A output-stage. To solve this problem, a feedforward transconductance stage (FTS) can be added to the amplifier [7], [10], as shown in Fig. 7. The current consumption of the modified amplifier becomes $(m+4k+8)I_B$.

In this structure, the second gain stage ($G_{m2}$) is implemented by a pMOSFET (i.e., $M_5$), and the FTS stage ($G_{mft1}$) is constructed using nMOSFET (i.e., $M_6$), and together, they form a push–pull output stage. Both $G_{m2}$ and $G_{mft1}$ are driven by two independent cascaded small-gain stages. $M_{X1}$ and $M_{X2}$ jointly supply $v_{in}$ to the FTS, since the signal voltage at $v_{D0}$ is given by $-g_{m1}(1/g_{m3})(g_{mX1})(1/g_{mX2})(v_{in})$, where $g_{m1}$, $g_{m3}$, $g_{mX1}$, and $g_{mX2}$ are the transconductances of $M_1$, $M_3$, $M_{X1}$, and $M_{X2}$, respectively. In this design, $(W/L)_F = 2(W/L)_N$ is selected to compensate the difference between $\mu P$ and $\mu N$, and hence, $g_{m1} = g_{m3} = g_{mX1} = g_{mX2}$, to give a gain of $-1$. Thus, $v_{D0} = -v_{in}$. In order to investigate the small-signal behavior of the amplifier in Fig. 7, the structure shown...
in Fig. 8 is studied. \(k_m\) and \(k_f\) are the wide-bandwidth scalars implemented by the two sets of small-gain stages, as shown in Fig. 7. This structure is basically the modified version of a two-stage SMC with FTS [7], [10].

By altering all \(G_{m2}\) terms to \(k_m G_{m2}\) and all \(G_{mf1}\) terms to \(k_f G_{mf1}\), the transfer function is given by [10]

\[
\frac{v_o(s)}{v_{in}(s)} \approx \frac{k_m G_{mf1} G_{m2} R_1 R_2 [1 + s C_m G_{m2} G_{mf1}]}{1 + s C_m R_1 R_2 (1 + s C_m G_{m2})}. \tag{13}
\]

Comparing (13) with (7), it is found that the dominant pole, nondominant pole, and GBW for a PM of about 60° remain the same as the expressions in (8), (9), and (11), respectively. The required \(C_m\) remains the same as the dimension condition stated in (12). The only difference is the zero, due to the FTS. Since \(k_f G_{mf1} > G_{m1}\), the left-half-plane (LHP) zero, \(z_{LHP}\), is given by

\[
z_{LHP} \approx \frac{G_{m1} k_m G_{m2}}{C_m k_f G_{mf1}}. \tag{14}
\]

Depending on its actual value, \(z_{LHP}\) can help to increase the PM of the amplifier. Using (8), (9), and (11) to analyze the SMC amplifier in Fig. 7, it is found that \(G_{m2} = g_{m5}\), \(G_{mf1} = g_{m6}\), and \(k_m = k_f = k^2\).

Fig. 9(a) and (b) is used to study the large-signal behavior of the two-stage SMC amplifier (see Fig. 7). When a rising step is applied to \(v_{IN+}\), \(M_1\), \(M_3\), and \(M_4\) are switched OFF, and \(v_{U0}\) is pulled low. The current comparator, formed by \(M_{U11}\) and \(M_{U13}\), pulls \(v_{U1}\) high, which in turn switches OFF \(M_{U12}\) and \(M_{U21}\). As a result, the drain current of \(M_{U22}\) is defined by \(M_{U23}\) only. With the \(m\)-times ratio of \(M_{U22}\) and \(M_5\), the transient current flowing through \(M_5\) is \(m(k + 1)I_B\). For the lower part of the circuit, since \(M_3\) is switched OFF, \(M_{X1}, M_{X2},\) and \(M_{D11}\) are all switched OFF. The current from \(M_{D13}\) flows into \(M_{D12}\). The current comparator, formed by \(M_{D21}\) and \(M_{D23}\), pulls \(v_{D2}\) low to shut down \(M_{D22}\) and \(M_6\). Thus, \(SR^+ = m(k + 1)I_B/C_O\).

Similarly, when a falling step is applied to \(v_{IN+}\), \(M_2\) is switched OFF, and \(v_{U0}\) is pull high to shut down \(M_{U11}\). The current of \(M_{U12}\) is defined as \(M_{U13}\) only. The current comparator, formed by \(M_{U21}\) and \(M_{U23}\), pulls \(v_{U2}\) high to shut down \(M_{U22}\) and \(M_5\). Since all tail current flows to \(M_1\), the current flowing through \(M_{X1}\) and \(M_{X2}\) is \(2I_B\). The current comparator, formed by \(M_{D11}\) and \(M_{D13}\), pulls \(v_{D1}\) low to shut down \(M_{D12}\) and \(M_{D21}\). The current from \(M_{D23}\) goes into \(M_{D22}\) and is then multiplied by \(m\) times to form the transient current of \(M_6\), which is equal to \(m(k + 1)I_B\). As a result, \(SR^- = m(k + 1)I_B/C_O\). This circuit structure enables symmetrical slewing on both the rising and the falling transient changes of \(v_O\).
The small-signal and large-signal performances of the SMC amplifier with small-gain stages and FTS in Fig. 7 are included in Table I. From Table I, it is evident that this amplifier has better GBW (increased by \( k^2 \) times) and SR [increased by about \( 2(k+1) \) times] than its counterparts shown in Figs. 2 and 5, whereas the current consumption is only linearly related to \( k \).

IV. PROPOSED AMPLIFIER STRUCTURE

The small-gain stages used in the SMC amplifier of Fig. 7 receive fixed bias currents from \( M_{U13}, M_{U23}, M_{D13}, \) and \( M_{D23} \), such that the resultant transient current is limited to \( m(k+1)I_B \). A simple modification to further improve the transient current is to replace the static bias points at the gates of \( M_{U13}, M_{U23}, M_{D13}, \) and \( M_{D23} \) (i.e., \( V_{B1} \) and \( V_{B2} \)) through dynamic nodes. Fig. 10 shows a modified circuit, which is the proposed cross-coupled structure of the small-gain stages.

In order to illustrate the SR improvement by the proposed connections, the transient responses are studied using Fig. 11(a) and (b). In Fig. 11(a), a rising step applied to \( v_{IN+} \) causes \( M_1, M_3, M_4, M_X1, \) and \( M_X2 \) to shut down, and consequently, \( M_{U11}, M_{U12}, M_{U13}, M_{U21}, M_{D11}, M_{D12}, M_{D22}, M_{D23}, \) and \( M_6 \) are then switched off. The transient current from \( M_5 \) is determined by the drain current of \( M_{D13} \) (i.e., \( i_{D13} \)), which is controlled by \( V_{U0} = v_{IN+} - V_{DS2} + V_{DS2} \), where \( V_{U0} \) is lower than \( V_{DD} - V_{GS3} \) under normal bias in Fig. 10. Thus, \( i_{D13} \) should be larger than \( (k+1)2I_B \). This current is further amplified by \( m(k+1) \) times via \( M_{D13}, M_{D22}, M_{D23}, \) and \( M_6 \), to achieve a \( M_{D13} \) drain current greater than \( 2m(k+1)^2I_B \). As a result, \( SR^+ \) is more than \( 2m(k+1)^2I_B/C_O \). Similarly, referring to Fig. 11(b) for the case with a falling step applied to \( v_{IN+} \), SR will cause a transient current of \( 2m(k+1)^2I_B \) to cause \( SR^- = 2m(k+1)^2I_B/C_O \). These results have been included in Table I. Compared with the transient response of an amplifier without the cross-coupled connections of the small-gain stage (Fig. 7), the SR is further improved by an additional \( (k+1) \) times.

Although the amplifier in Fig. 10 contains a second gain stage and an FTS, the same as the structure in Fig. 8, the effective \( G_{m2} \) and \( G_{mf1} \) of this circuit cannot be obtained by inspection, since there are many interactions among the four small-gain stages. In order to evaluate the effective \( G_{m2} \) and \( G_{mf1} \), the signal flow from \( V_{U0} \) and \( V_{D0} \) to \( v_o \) for the amplifier in Fig. 10 is shown in Fig. 12. The transconductances of all pMOSFETs and nMOSFETs are simply defined as \( g_{mp} \) and \( g_{mn} \). To simplify the analysis and as per before, let \( g_{mp} = g_{mn} \) through setting \( (W/L)_p = 2(W/L)_n \). From Fig. 12 and the Appendix, it is found that

\[
v_o = \left\{\begin{array}{l}
-\{(2k^2 + 2k + 1)g_{m5} + 2(k+1)g_{m6}\}V_{U0}

-\{(2k+1)g_{m5} + (2k^2 + 2k + 1)g_{m6}\}V_{D0}
\end{array}\right\} \left(\frac{r_{o5}}{r_{o6}}\right).
\]

Hence, \( k_mG_{m2} = (2k^2 + 2k + 1)g_{m5} + 2(k+1)g_{m6} \) and \( k_fG_{mf1} = 2k(k+1)g_{m5} + (2k^2 + 2k + 1)g_{m6} \). If \( k = 2 \) is
Fig. 13. Full circuit diagram of the proposed amplifier with 12-stages of cross-coupled small-gain stages and FTS.

Fig. 14. Signal flow of the proposed amplifier of Fig. 13, from \(v_{u0}\) and \(v_{d0}\) to \(v_o\).

TABLE II

<table>
<thead>
<tr>
<th>Amplifier</th>
<th>Gain</th>
<th>(p_2)</th>
<th>GBW</th>
<th>PM</th>
<th>SR</th>
<th>I_{DD}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig. 2</td>
<td>(g_m G_m)</td>
<td>(g_m G_m)</td>
<td>(0.5 g_m G_m)</td>
<td>(&lt;60^\circ)</td>
<td>((i_{N2} - 20 I_B)/C_O)</td>
<td>(20 I_B/C_O)</td>
</tr>
<tr>
<td>Fig. 5</td>
<td>(4 g_m G_m)</td>
<td>(4 g_m G_m)</td>
<td>(2 g_m G_m)</td>
<td>(&gt;60^\circ)</td>
<td>(40 I_B/C_O)</td>
<td>(20 I_B/C_O)</td>
</tr>
<tr>
<td>Fig. 7</td>
<td>(-4 g_m G_m)</td>
<td>(4 g_m G_m)</td>
<td>(2 g_m G_m)</td>
<td>(&gt;60^\circ)</td>
<td>(60 I_B/C_O)</td>
<td>(60 I_B/C_O)</td>
</tr>
<tr>
<td>Fig. 10</td>
<td>(-64 g_m G_m)</td>
<td>(7812 g_m G_m)</td>
<td>(3906 g_m G_m)</td>
<td>(&gt;60^\circ)</td>
<td>(&gt;29160 I_B/C_O)</td>
<td>(29160 I_B/C_O)</td>
</tr>
<tr>
<td>Fig. 13</td>
<td>(-64 g_m G_m)</td>
<td>(7812 g_m G_m)</td>
<td>(3906 g_m G_m)</td>
<td>(&gt;60^\circ)</td>
<td>(&gt;29160 I_B/C_O)</td>
<td>(29160 I_B/C_O)</td>
</tr>
</tbody>
</table>

selected, \(k_m G_m = 13 g_m + 12 g_m\) and \(k_f G_m = 12 g_m + 13 g_m\). Using \(9\), \(p_2 = k_m G_m + 1/2 + 1/2 g_m + 2k(k + 1) g_m + g_m^2 + 2(k + 1) g_m + 1/2 g_m^2\) for a PM of more than \(60^\circ\) due to the presence of an LHP zero. It is noted that the current consumption is only \((m + 4k + 8) I_B\). The performance results are again included in Table I.

From the previous discussions and Table I, it is concluded that the amplifier structure in Fig. 10 provides much better GBW and SR. When more small-gain stages are used, the resultant GBW and SR can be substantially enhanced. Thus, a two-stage SMC amplifier with 12 small-gain stages and FTS is proposed and shown in Fig. 13. Low-voltage cascode structure can be used for further enhancement to the current matching. Based on the previous study, the SR of this amplifier is given by

\[
SR \approx \frac{2m (k + 1)^6 I_B}{C_O}.
\]

For the selected values of \(k = 2\) and \(m = 20\), SR = \(29160 I_B/C_O\). For the small-signal response, the signal flow of the proposed amplifier is shown in Fig. 14. From the Appendix, it is found that

\[
v_o = (-k_m G_m v_{u0} - k_f G_m v_{d0}) \frac{r_{ds}}{r_{ds}}
\]

where \(k_m G_m \approx k_f G_m \approx (32k^6 + 96k^5 + 120k^4 + 80k^3 + 30k^2 + 6k) g_m + g_m^2\). In this design, \(k = 2\) is selected to give

\[
\text{GBW} = \frac{3906 (g_m + g_m)}{C_O}
\]

for a PM of \(60^\circ\). The improvement factor is 3906, and both \(M_5\) and \(M_6\) contribute to the GBW. From (14), \(z_{LHP} = G_m / C_m\). It is noted that the required \(C_m\), according to (12), is significantly reduced. The above results have been included in Table I.

Based on Table I, Table II shows the GBW, SR, and \(I_{DD}\) when \(k = 2\) and \(m = 20\) are selected. The selection of \(k = 2\) is to avoid large gate capacitance at nodes \(v_{U5}\) and \(v_{D5}\), so that both nodes, with a node resistance of \(1/g_m\), are of low impedances. As for \(m = 20\), it is used to enhance the driving capability of the output stage formed
by $M_5$ and $M_6$. The bias conditions of $M_1$, $M_2$, $M_3$, $M_4$, $M_5$, and $M_6$ are the same, such that their transconductances and drain resistances have no difference in all five circuits under investigation. Table II clearly shows that the proposed amplifier in Fig. 13 has much better GBW and SR, so that the improvements in GBW and SR outweigh the slight increase of $I_{DD}$. Finally, the proposed structure can be easily altered to either increase or reduce on the number of small-gain stages, systematically, without necessitating complex changes.

The proposed amplifier structure shown in Fig. 13 contains multiple current mirrors. In order to investigate the effect due to device mismatches, Monte Carlo simulation of one million samples has been conducted. In this simulation, the worst-case variations of the drain currents of all transistors are $\pm 20\%$. In particular, the drain currents of $M_{U1}, M_{U2}, M_{D11}$ and $M_{D12}$ are selected, and the distributions of the one million samples are shown in Fig. 15(a). The distribution of the offset voltage of the amplifier under the same condition is shown in Fig. 15(b), and it clearly shows that the offset voltage is within $\pm 15$ mV, respectively.

As a matter of fact, one concern of the proposed cross-coupled small-gain stage is device matching. For example, when $M_{U1}$ and $M_{U2}$ have a mismatch of $\pm 20\%$, which is considered as the worst case, the drain current of $M_{U2}$ may be smaller. With the more potential mismatches between $M_{U1}$ and $M_{U2}$, and then $M_{U1}$ and $M_{U2}$, and so on, it results in a serious drift of drain currents on both $M_{U1}$ and $M_{U2}$. The drain current of $M_{U2}$ may go to zero, and proper dc bias cannot be established. From Fig. 15(b), it clearly shows that the drain currents of $M_{U2}$ and $M_{D12}$ may be as small as $0.2 \mu A$. Therefore, the device-mismatch effect should be considered, when selecting more cross-coupled small-gain stages. In the proposed design, the closely packed interdigitized layout is used to further minimize the mismatch.

Similar to a generic multistage amplifier, the equivalent input referred noise of the proposed amplifier is mainly due to the input stage [24], [25]. However, additional noises from $M_{X1}$, $M_{X2}$, $M_{U13}$, and $M_{D11}$ go into the input stage because of the low-impedance connection at the gates of $M_3$ and $M_4$. Thus, the equivalent input referred noise, $v_{\text{inn}}^2$, can be approximately given by [24], [25]

$$v_{\text{inn}}^2 \approx v_{n1}^2 + v_{n2}^2 + \frac{g_{m3}}{g_{m1}} \cdot v_{n3}^2 + v_{n4}^2 + v_{nX1}^2 + v_{nX2}^2 + v_{nD11}^2 + v_{nU13}^2 \times g_{m1}^{-2}$$

(19)

where $v_{n1}, v_{n2}, v_{n3}, v_{n4}, v_{nX1}, v_{nX2}, v_{nD11},$ and $v_{nU13}$ are the equivalent noises due to the flicker noise and channel noise appearing at the gate of $M_1$, $M_2$, $M_3$, $M_4$, $M_{X1}$, $M_{X2}$, $M_{D11}$, and $M_{U13}$, respectively. Equivalent input referred noise can be reduced by selecting nMOSFET to implement the differential pair and pMOSFET as the active load, such that $g_{m3}$ is less than $g_{m1}$ for reducing the noises from the active load and the cross-coupled small-gain stages.

V. EXPERIMENTAL RESULTS

The proposed amplifier shown in Fig. 13 is implemented in UMC 0.13-\(\mu\)m CMOS technology ($V_{\text{THN}} = 0.38$ V and $V_{\text{THP}} = -0.33$ V). Only standard-\(V_{\text{TH}}\) devices are used in this design. The chip micrograph is given in Fig. 16, and the active chip area is 0.0056 \(\text{mm}^2\). A 1.62-pF on-chip compensation capacitor (i.e., $C_m$ in Fig. 13) is used in this design.

Fig. 16. Micrograph of the proposed amplifier.
The supply voltage is 0.7 V, and the current consumption is 20 μA. Two samples have been measured. The measured offset voltages are 1.5 and 2.4 mV.

The low-frequency gain is about 100 dB. Three cases of capacitive loads, $C_O = 9.5$, 14.4, and 18.9 nF (the measured values of the capacitors), are considered. The measured open-loop frequency responses are shown in Fig. 17. The zoomed-in view of the responses around the GBW is provided in Fig. 18. The GBWs and PMs for $C_O = 9.5$, 14.4, and 18.9 nF are 1.17 MHz and 74.8°, 0.982 MHz and 62.2°, and 0.856 MHz and 58.6°, respectively.

The measured SRs of the proposed amplifier in unity-gain configuration with a 0.3 V step applied are shown in Fig. 19(a). The average SRs for $C_O = 9.5$, 14.4, and 18.9 nF are 0.3679, 0.3263, and 0.2853 V/μs, respectively. The step responses reflect exponential characteristics due to large PM, while there is a slight overshoot for the case of $C_O = 18.9$ nF. Two more transient measurements with $C_O = 9.5$ nF are shown in Fig. 19(b) and (c). Fig. 19(b) shows the response when a very small step input (20 mV) is applied to the amplifier in unity-gain configuration, while Fig. 19(c) shows the response when a 0.15 V step is applied to the amplifier with a closed-loop gain of 2 V/V.

The improvements in both the GBW and the SR are basically due to the fact that the proposed structure enables much larger improvement factors for the GBW and the SR, as shown in (16) and (18). The static current consumption is low.
TABLE III

PERFORMANCE COMPARISON

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS technology (μm)</td>
<td>0.35</td>
<td>0.065</td>
<td>0.35</td>
<td>0.13</td>
<td>0.13</td>
</tr>
<tr>
<td>Chip area (mm²)</td>
<td>0.02</td>
<td>0.0088</td>
<td>0.016</td>
<td>0.0032</td>
<td>0.0056 (94.49 μm × 59.45 μm)</td>
</tr>
<tr>
<td>Cₒ (pF)</td>
<td>150</td>
<td>500</td>
<td>15000</td>
<td>680</td>
<td>9500</td>
</tr>
<tr>
<td>Vₒ (V)</td>
<td>1.5</td>
<td>1.2</td>
<td>2</td>
<td>1.2</td>
<td>0.7</td>
</tr>
<tr>
<td>Iₒ (nA)</td>
<td>20</td>
<td>17</td>
<td>72</td>
<td>10.5</td>
<td>20</td>
</tr>
<tr>
<td>dc gain (dB)</td>
<td>110</td>
<td>&gt;100</td>
<td>&gt;100</td>
<td>&gt;100</td>
<td>~100</td>
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<tr>
<td>GBW (MHz)</td>
<td>4.4</td>
<td>2</td>
<td>0.95</td>
<td>3.37</td>
<td>1.17</td>
</tr>
<tr>
<td>PM (°)</td>
<td>57</td>
<td>52</td>
<td>52.3</td>
<td>45</td>
<td>74.8</td>
</tr>
<tr>
<td>SR (V/μs)</td>
<td>1.8</td>
<td>0.65</td>
<td>0.22</td>
<td>0.67</td>
<td>0.3679</td>
</tr>
<tr>
<td>On-chip capacitance (pF)</td>
<td>1.6</td>
<td>1.15</td>
<td>2.6</td>
<td>0.587</td>
<td>1.62</td>
</tr>
<tr>
<td>FOMs (MHz·pF/mW)</td>
<td>22000</td>
<td>49020</td>
<td>98958</td>
<td>180157</td>
<td>796680</td>
</tr>
<tr>
<td>FOMt (V·μs·pF/mW)</td>
<td>9000</td>
<td>15931</td>
<td>22917</td>
<td>35550</td>
<td>249654</td>
</tr>
<tr>
<td>IFOMs (MHz·pF/μA)</td>
<td>33000</td>
<td>58823</td>
<td>197916</td>
<td>216188</td>
<td>557676</td>
</tr>
<tr>
<td>IFOMt (V·μs·pF/μA)</td>
<td>13500</td>
<td>19118</td>
<td>45834</td>
<td>42660</td>
<td>174758</td>
</tr>
<tr>
<td>LC-FOMs (MHz/mW)</td>
<td>13750</td>
<td>42626</td>
<td>38061</td>
<td>306911</td>
<td>491777</td>
</tr>
<tr>
<td>LC-FOMt (V·μs/mW)</td>
<td>5625</td>
<td>13853</td>
<td>8814</td>
<td>60562</td>
<td>154107</td>
</tr>
</tbody>
</table>

Furthermore, with Cₒ = 14.4 nF, the measured power-supply rejection ratio of Vₒ/ΔV, at 10 and 100 kHz is 69.04/72.85 and 37.99/36.66 dB, respectively. The total harmonic distortions had been measured with a 300-mV sinusoidal wave inputted to the amplifier in unity-gain configuration. As shown in Fig. 20, they are −44.61 dBc at 10 kHz, −27.34 dBc at 100 kHz, and −26.49 dBc at 1 MHz.

Comparing the proposed amplifier with the prior arts that were stabilized by different compensation topologies, the well-accepted figure-of-merits for the small-signal and large-signal performances have been used. They include FOMₛ, FOMₗ, IFOMₛ, and IFOMₗ [8]–[20], as well as LC-FOMₛ and LC-FOMₗ [15] that are related to the on-chip capacitor consideration. A larger value on the figure-of-merit basically reflects a better compensation topology. From the performance summary of the proposed and the state-of-the-art amplifiers in Table III, it is clear that the proposed amplifier has substantially outperformed the others (comparisons using the best results: 1) FOMₛ: 6.4 times; 2) FOMₗ: 10.8 times; 3) IFOMₛ: 3.7 times; 4) IFOMₗ: 5.9 times; 5) LC-FOMₛ: 2.3 times; and 6) LC-FOMₗ: 3.9 times) in both the small-signal and large-signal domains. It is noted that the supply voltage of the proposed amplifier is the lowest (without using low-Vᵣ devices), and this reveals that the proposed cross-coupled small-gain-stage structure is suitable for ultralow-voltage designs. This feature may not be possible in other state-of-the-art designs, since some of them make use of cascode structures to construct current buffers.

VI. CONCLUSION

A structure of the two-stage SMC large-capacitive-load amplifier with multiple cross-coupled small-gain stages has been introduced in this paper. Both small-signal and large-signal performances have been analyzed and proved by experimental results. Compared with the state-of-the-art designs, the proposed amplifier significantly shows better performances in both small-signal and large-signal domains, and the increase in current consumption is marginal. The structure can be systematically modified by increasing or reducing the required number of small-gain stages.

APPENDIX

DERIVATION OF THE EFFECTIVE TRANSCONDUCTANCE OF THE PROPOSED SECOND GAIN STAGE

The signal-flow graphs in Fig. 12 (i.e., the 4-small-gain-stage case) and Fig. 14 (i.e., the 12-small-gain-stage case) are used to evaluate the effective transconductances of the proposed small-gain stage and FTS. In order to estimate the effective transconductance, the relationships between a node and its preceding nodes need to be investigated, which can be given by

$$v_{u(i+1)} = \frac{-k_{mp}v_{ui} - (k + 1)g_{mn}v_{di}}{g_{mp}}$$

$$v_{d(i+1)} = \frac{-k_{mn}v_{di} - (k + 1)g_{mp}v_{ui}}{g_{mn}}$$

(A.1)  

(A.2)
where $i \geq 0$ corresponds to the sequential numbers of nodes. When $g_{mn} = g_{imp}$, (A.1) and (A.2) can be simplified to
\[
v_{u(i+1)} = -[kv_{ui} + (k + 1)v_{di}] \quad (A.3)
\]
\[
v_{d(i+1)} = -[kv_{di} + (k + 1)v_{ui}] \quad (A.4)
\]
Subsequently
\[
v_{u(i+2)} = -[kv_{ui} + (k + 1)v_{di} + (1 + k)v_{di}] = -k[v_{ui} + (k + 1)v_{di} + (1 + k)v_{di}] = k^2v_{ui} + k(k + 1)v_{di} + k(1 + k)v_{di} + (1 + k)^2v_{ui} = [k^2 + (k + 1)^2]v_{ui} + 2k(1 + k)v_{di} = (2k^2 + 2k + 1)v_{ui} + (2k^2 + 2k)v_{di} \quad (A.5)
\]
which leads to $v_{u2} = (2k^2 + 2k)v_{u0} + (2k^2 + 2k)v_{d0}$. Similarly, in the feedforward path
\[
v_{d(i+2)} = (2k^2 + 2k + 1)v_{d0} + (2k^2 + 2k)v_{d0} \quad (A.6)
\]
Hence, $v_{d2} = (2k^2 + 2k + 1)v_{d0} + (2k^2 + 2k)v_{d0}$, whereas the output voltage is
\[
v_{o} = [v_{u2} (-g_{m5}) + v_{d2} (-g_{m6})] (r_{os} / r_{o6}) \quad (A.7)
\]
Substituting the expressions of $v_{u2}$ and $v_{d2}$ with respect to $v_{u0}$ and $v_{d0}$ into (A.7) gives
\[
v_{o} = [2(2k^2 + 2k + 1)v_{u0} + 2(k^2 + 2k)v_{d0}] (r_{os} / r_{o6}) (A.8)
\]
which is exactly (15). As a result, signal at $v_{o0}$ is amplified by $[(2k^2 + 2k + 1)g_{m5} + 2k(k + 1)g_{m6}] (r_{os} / r_{o6})$ when it reaches $v_{o6}$. Signal at $v_{d0}$ has $2k(k + 1)g_{m5} + 2k^2 + 2k + 1]g_{m6}] (r_{os} / r_{o6})$ times of amplification, which equivalently suggests that the effective transconductances are $k_m G_m = 2(2k^2 + 2k + 1)g_{m5} + 2\alpha(k + 1)g_{m6}$ and $k_f G_{mf} = 2(k + 1)g_{m6} + 2k^2 + 2k + 1]g_{m6}$ for the second stage and the FTS, respectively.

Likewise, the effective transconductances of the 12-small-gain stage case in Fig. 14 can be calculated using (A.5) and (A.6), as
\[
v_{u6} = (2k^2 + 2k + 1)v_{u4} + (2k^2 + 2k)v_{d4} = [(2k^2 + 2k + 1)v_{u2} + (2k^2 + 2k)v_{d2}] + (2k^2 + 2k)(2k^2 + 2k + 1)v_{u2} + (2k^2 + 2k)v_{d2} = [(2k^2 + 2k + 1)^2 + (2k^2 + 2k)v_{u2} + (2k^2 + 2k + 1)v_{d2} = [(K + 1) + K^2]v_{u2} + 2K(K + 1)v_{d2} \quad (A.9)
\]
where $K = 2k^2 + 2k$. Substituting the expressions of $v_{u2}$ and $v_{d2}$ into (A.9), it attains
\[
v_{u6} = [(K + 1)^2 + K^2](K + 1) + 2K^2(K + 1)v_{u0} + 2K^2 + K^2]v_{d0} = 4K^3 + 6K^2 + 3K + 1)v_{u0} + (4K^3 + 6K^2 + 3K)v_{d0} = (\alpha + 1)v_{u0} + \alpha v_{d0} \quad (A.10)
\]
where $\alpha = 4K^3 + 6K^2 + 3K = 32K^6 + 96K^5 + 120K^4 + 80K^3 + 30K^2 + 6K$, while
\[
v_{d6} = (\alpha + 1)v_{d0} + \alpha v_{d0} \quad (A.11)
\]
is derived in the same way. Therefore, for the 12-stage case
\[
v_{o} = \begin{cases} -[\alpha + 1)v_{u0} + \alpha v_{d0}]g_{m5} & (r_{os} / r_{o6}) \\ -[\alpha + 1)v_{u0} + \alpha v_{d0}]g_{m6} & (r_{os} / r_{o6}) \\ -[\alpha + 1)v_{u0} + \alpha v_{d0}]v_{d0} & (r_{os} / r_{o6}) \end{cases} \quad (A.12)
\]
where $k_m G_m = (\alpha + 1)g_{m5} + \alpha g_{m6}$ and $k_f G_{mf} = (\alpha + 1)g_{m6}$ are the effective transconductances of the second stage and the feedforward stage, respectively. Furthermore, since $\alpha = 32K^6 + 96K^5 + 120K^4 + 80K^3 + 30K^2 + 6K$ is very large (even for $k = 1, \alpha$ is much larger than 1), it can be approximated that $k_m G_m \approx k_f G_{mf} \approx \alpha (g_{m5} + g_{m6}) = (32K^6 + 96K^5 + 120K^4 + 80K^3 + 30K^2 + 6K)(g_{m5} + g_{m6})$, insinuating not only that both the second gain stage and the FTS are enhanced by a factor of $\alpha$, but also that both $M_5$ and $M_6$ contribute to the GBW, as shown in (18).

REFERENCES
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