A CMOS Low-Dropout Regulator With Dominant-Pole Substitution

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Abstract—A dominant-pole substitution (DPS) technique for low-dropout regulator (LDO) is proposed in this paper. The DPS technique involves signal-current feedforward and amplification such that an ultralow-frequency zero is generated to cancel the dominant pole of LDO, while a higher frequency pole substitutes in and becomes the new dominant pole. With DPS, the loop bandwidth of the proposed LDO can be significantly extended, while a standard value and large output capacitor for transient purpose can still be used. The resultant LDO benefits from both the fast response time due to the wide loop bandwidth and the large charge reservoir from the output capacitor to achieve the significant enhancement in the dynamic performances. Implemented with a commercial 0.18-μm CMOS technology, the proposed LDO with DPS is validated to be capable of delivering 100 mA at 1.0-V output from a 1.2-V supply, with current efficiency of 99.86%. Experimental results also show that the error voltage at the output undergoing 100 mA of load transient in 10-ns edge time is about 25 mV. Line transient responses reveal that no more than 20-mV instantaneous changes at the output when the supply voltage swings between 1.2 and 1.8 V in 100 ns. The power-supply rejection ratio at 3 MHz is −47 dB.

Index Terms—Dominant pole, low-dropout regulator (LDO), zero generation.

I. INTRODUCTION

LOW-DROPOUT regulator (LDO) typically employs a large output capacitor \(C_O\) with a small equivalent series resistance (ESR) to achieve closed-loop stability and small transient errors [1]–[10]. The strategy to achieve stability assurance is the dominant-pole frequency compensation (DPFC), which is most suited for LDOs since a LDO should have null signal at its output. This calls for the \(C_O\) to be as large as possible. But the values of off-chip components on PCB should not be overdesigned for the ultrathin modern portable electronic devices. Also, an insufficiently large \(C_O\) is not reliable enough to maintain the capacitor voltage, i.e., the output voltage of LDO. The DPFC scheme, therefore, serves to increase the LDO response time to degrade the transient responses of the LDO.

To extend the LDO loop bandwidth, researchers proposed to cancel the dominant pole by creating an ultralow-frequency left-half-plane (LHP) zero [11]. A large capacitor and resistor are generally needed to create this zero, and more importantly, another low-frequency pole is naturally generated due to the additional resistance that increases the impedance of the circuit nodes [11]. In order to create a zero without generating a pole, a current-mode approach was proposed [12]. Though the method is effective in creating a stand-alone zero, it is very difficult to locate the zero at ultralow frequency since a high gain, i.e., ratio of output and input currents, is mandatory and, hence, additional current consumption.

In this paper, a dominant-pole substitution (DPS) technique for LDO is proposed. The proposed method enables that the feedback signal has an additional path to skip the error amplifier (EA) in LDO to control the power transistor directly to achieve faster response. The proposed DPS technique and the related circuit implementation are covered in Section II. In Section III, the experimental results of the proposed LDO design is reported. Last, the conclusion of this paper is provided in Section IV.

II. PROPOSED LDO WITH DPS

The concept of the proposed LDO can be explained using Fig. 1. The input voltage, reference voltage, output voltage, and output current are denoted by \(V_{IN}\), \(V_{REF}\), \(V_O\), and \(I_O\), respectively. The output capacitor \(C_O\) has an ESR of \(R_E\). A current source is connected at \(V_O\) to model the load. \(R_{F1}\) and \(R_{F2}\) are feedback resistors to define the feedback factor \(\beta = R_{F2}/(R_{F1} + R_{F2})\). \(M_P\) is the power PMOS transistor, and its gate capacitance is explicitly indicated in Fig. 1 and denoted as \(C_{gs}\). \(R_{oa}\) is the output resistance of the EA. The response time of an LDO is limited by the EA. In this paper, a new LDO structure with \(V_O\) feedforward is proposed. With this feedforward circuit, the change of \(V_O\) will be propagated directly to the gate of \(M_P\) for fast and direct regulation. In order to realize this concept, the transconductance cell of the EA was modified to incorporate a \(V_{IN}\)-feedforward feature, which yields a triple-input EA. The...
proposed transconductance cell and triple-input EA will first be described in this section. Thereafter, the proposed LDO using the two circuit techniques to achieve DPS will be presented.

A. Proposed Transconductance Cell

Fig. 2(a) shows the proposed transconductance cell. The supply voltage is $V_{IN}$, which is also the input voltage of the proposed LDO. $I_B$ is the bias current. $M_{B1}$ forms current mirrors with $M_{B2}$, $M_{B3}$, and $M_{B4}$, with current ratios of 1:1, 1 : (1 + $k_1$), 1 : (1 + $k_2$), and 1 : (1 + $k_3$), respectively, as defined by the aspect size ratios of the PMOS transistors above the supply line in Fig. 2(a). Note that $k_1$, $k_2$, and $k_3$ are all larger than 1 in this design. The lower part of the circuit is formed by $M_{N1}$, $M_{N2}$, $M_{N3}$, $M_{N4}$, $M_{N5}$, and $M_{N6}$, with size ratios of 1 : $k_1$ : 1 : $k_2$ : 1 : $k_3$. The bias currents from $M_{B2}$, $M_{B3}$, $M_{B4}$, and $M_{B5}$ are distributed to the NMOS transistors according to their size ratios. An on-chip capacitor $C_X$ is connected to the diode-connected point of $M_{N1}$ [16], such that the source of the test voltage signal $v_{test}$ sees an input impedance of $1/sC_X + 1/g_{mn}$. As a result, the input current of this circuit $i_x$ is given by

$$i_x = \frac{v_{test}}{1/sC_X + 1/g_{mn}} = \left( \frac{sC_X}{1 + sC_X/g_{mn}} \right) v_{test}. \quad (1)$$

$i_x$ is injected into the diode-connected point of $M_{N1}$ where it becomes $k_1i_x$ at $M_{N2}$, $k_1k_2i_x$ at $M_{N4}$, and finally, $k_1k_2k_3i_x$ at $M_{N6}$. It is noted that the signal currents are not affected by $M_{B2}$, $M_{B3}$, $M_{B4}$, and $M_{B5}$ as the PMOS transistors only provide fixed bias currents. The current gain of the proposed circuit is $k_1k_2k_3$, which is a product of three factors. The total supply current is simply the sum of the three factors ($k_1 + k_2 + k_3 + 5)I_B$. Moreover, the impedances of the nodes seen by the signal are low due to the diode-connected structures. Thus, the output current $i_{ox}$ is simply equal to

$$i_{ox} = k_1k_2k_3i_x = s \left( \frac{k_1k_2k_3C_X}{1 + sC_X/g_{mn}} \right) v_{test}. \quad (2)$$

From (2), it is evident that $i_{ox}$ leads $v_{test}$ by at most $90^\circ$ within the bandwidth of $g_{mn}/C_X$. Moreover, the transconductance of the proposed circuit is large owing to the factor of $k_1k_2k_3$.

B. Proposed Triple-Input EA

Fig. 1(b) shows the proposed triple-input EA, which is used in the proposed LDO with DPS. The three inputs are as follows:

1) at the gate of $M_1$, with input $\beta v_{test}$, where $\beta = R_{F2}/(R_{F1} + R_{F2})$, and $R_{F1}$ and $R_{F2}$ are the feedback resistors of the proposed LDO shown in Fig. 3;

2) at the gate of $M_2$, with reference voltage, $V_{REF}$, supplied by a reference circuit. It is noted that $V_{REF}$ is a dc voltage and is also the ac ground;

3) at the input of the proposed transconductance cell in Fig. 2(a), with an input signal of $v_{test}$.

The input differential pair $M_1$ and $M_2$ generates a small-signal current $i_a = 0.5 g_{m1}\beta v_{test}$ where $g_{m1}$ is the transconductance of $M_1$, as indicated in Fig. 2(b). Similar to the proposed transconductance cell in Fig. 2(a), this current is increased by a factor of $k_5$ at $M_4$ (and also $M_5$), and further amplified to $k_4k_5i_a$ at $M_{10}$ and $M_{12}$. The small-signal output current due to $M_1$ and $M_2$ becomes $2k_4k_5i_a$, which is equal to $k_4k_5g_{m1}\beta v_{test}$.

Moreover, the proposed transconductance cell shown in Fig. 2(a) is connected to the diode-connected point of $M_{11}$ in Fig. 2(b). The current mirror formed by $M_{11}$ and $M_{12}$ further increases the output signal current from the transconductance cell by $k_4$ times. As a result, the total small-signal output current $i_{oa}$ of this triple-input EA is

$$i_{oa} = k_4k_5g_{m1}\beta v_{test} + k_4k_2k_3k_4i_a = k_4k_5g_{m1}\beta v_{test} + s \left( \frac{k_1k_2k_3k_4C_X}{1 + sC_X/g_{mn}} \right) v_{test} = G_{ma}\beta v_{test} + \gamma v_{test} \quad (3)$$

where $G_{ma} = k_4k_5g_{m1}$ and $\gamma = k_1k_2k_3k_4C_X/(1 + sC_X/g_{mn})$, respectively. With a boosted effective transconductance of $G_{ma}$, $R_{oa}$ is no longer required to be very large and yet to obtain a reasonable voltage gain of the EA to assure good line and load regulations in the proposed LDO. When $R_{oa}$ is mediocre, the related pole will not be at a very low frequency. When an ESR zero is used to cancel this pole, the high-frequency power-supply rejection ratio (PSRR) can be improved [14] due to a small ESR.

C. Proposed LDO With DPS

The proposed LDO with DPS structure is shown in Fig. 3. The major difference of the proposed LDO structure from the conventional counterparts is the EA design. In this LDO, the proposed triple-input EA is employed. The inverting input is connected to a reference circuit. One of the two noninverting inputs is connected to the feedback resistors, and the other noninverting input is connected directly to $V_O$. In order to analyze the loop-gain response, the connection between the feedback resistors and $V_O$ is conceptually disconnected. Since the output node is connected with a large $C_O$, the disconnection for loop-gain analysis has less influence since there is only a slight change of nodal capacitance from the feedback resistors and the inputs of the EA. A test signal $v_{test}$ is injected at $R_{F1}$ and the feedback signal $v_{fb}$ is directly obtained from $V_O$. The ratio of $v_{fb}$ and $v_{test}$ (i.e., $v_{fb}/v_{test}$) is the transfer
Based on Fig. 3 and (3), the preliminary transfer function can be found and is illustrated graphically in Fig. 4(a). The test signal is fed into the triple-input EA to generate the small-signal output current given by (3). Since $R_{oa}$ and $C_{gp}$ are located at the output of the EA, an LHP pole given by $1/(C_{gp}R_{oa})$ is associated to the EA. Thereafter, the transfer function of the power stage formed by $M_P$, $C_O$, and $R_E$ is considered. In this part, $r_{op}$ represents the drain resistance of $M_P$, and it is dominant since $R_{F1}$ and $R_{F2}$ are generally much larger than $r_{op}$ [1], [2]. Both $C_O$ and $R_{F1}$ and $R_{F2}$ create an LHP pole (known as ESR pole) given by $1/(C_O R_{F1})$ [1]–[14]. Typically, the output pole cannot be rightly cancelled by the ESR zero since $r_{op}$ and $R_E$ are in vastly different orders of magnitude. The only possibility is when $R_E$ is much larger than $r_{op}$, where both output pole and ESR zero are in the same frequency location [15]. However, a large $R_E$ causes inferior transient response in terms of large output spike, which is generally not preferred [1], [6], [8].

Fig. 4(b) shows that the identical transfer function with $\gamma$ explicitly expressed. The final form of the transfer function is shown in Fig. 4(c). The proposed DPS has been clearly stated in Fig. 4(c), which consists of dominant-pole cancellation, non-dominant pole cancellation, and newly created dominant pole.
Given below is a summary of the proposed compensation approach.

1) Dominant-pole cancellation—The original dominant pole is the LDO output pole, i.e., $1/(C_O R_{op})$. The proposed transconductance cell creates a signal-current feedforward path to skip the EA core, thereby creating an ultralow-frequency zero $z_{ulf}$ given by

$$z_{ulf} = -\frac{\beta k_3 g_{m1}}{k_1 k_2 k_3 C_X}.$$ (4)

This zero is used to cancel the dominant pole. Due to the product of $k_1$, $k_2$, and $k_3$, the zero can be easily located to a very low frequency without the need for large resistance. $C_X$ can also be viewed as a multiplied capacitance, but the effect is to create a zero and not a pole, which is the main difference as compared to existing capacitance multiplier technique reported in [16]. Finally, it is noted that the factor $k_4$ does not exist in the relationship of $z_{ulf}$.

2) Nondominant pole cancellation—The nondominant pole is the pole at the EA’s output, i.e., $1/(C_{gp} R_{oa})$. This pole can be cancelled by the ESR zero $1/(C_O R_E)$. In the design of the triple-input EA, the effective transconductance of the part by $M_{1} - M_{12} G_{ma}$ is a boosted version of $g_{m1}$ with a factor of $k_1 k_3$. The boosted $G_{ma}$ enables the possibility of using a small $R_{oa}$ to achieve a reasonably high voltage gain of the EA. Thus, the size of $M_{10}$ and $M_{12}$ is selected to be $k_3$ times larger in order to reduce $R_{oa}$ and to increase the drain currents to improve the slewing speed at the gate of $M_P$. The smaller $R_{oa}$ causes the EA output pole to be shifted to a higher frequency so that a smaller $R_E$ can be used to achieve pole-zero cancellation. Furthermore, the small $R_E$ can reduce the amplitudes of overshoots and undershoots in the transient responses [1], [3], [8], as well as improve the PSRR at the high-frequency region [14].

3) Newly created dominant pole—The new dominant pole is given by $g_{mn}/C_X$, where $g_{mn}$ and $C_X$ are both designable. Theoretically, the rough estimation of the new unity-gain frequency (UGF) of the proposed LDO can be easily determined using the gain-bandwidth product relationship, assuming the effects due to the two pole-zero cancellations are negligible. It is given by

$$\text{UGF} = \left(\frac{\beta g_{ma} R_{oa} g_{mp} r_{op}}{1 + s C_X / g_{mn}}\right) \left(\frac{g_{mn}}{C_X}\right).$$ (5)

From (5), it can be noted that when the dominant pole is cancelled by the zero generated by the proposed circuits, the new UGF is a function of $g_{mn}/C_X$, which is the new dominant pole located at a higher frequency. Therefore, the loop bandwidth of the LDO with DPS is wider, so that faster transient responses can be achieved. The only limitation of the new UGF of the loop-gain response is the parasitic poles and zeros generated in the triple-input EA.

D. Simulated Results of the Proposed LDO With DPS

In order to evaluate the performance of the proposed LDO structure with DPS, the LDO in Fig. 3 with the auxiliary circuits...
in Figs. 1 and 2 is designed using the standard NMOS and PMOS transistor models provided by UMC 0.18-\textmu m CMOS technology. The range of $V_{\text{IN}}$ is between 1.2 and 1.8 V, and the preset $V_{\text{O}}$ is of 1 V. The maximum $I_{\text{O}}$ is 100 mA. An output capacitor of 1 \textmu F with ESR of 0.35 \textOmega is used in this design. The unit sizes of the NMOS and PMOS transistors are selected to be 3 \mu m/0.5 \mu m and 6 \mu m/0.5 \mu m, respectively. The aspect ratio of $M_{\text{P}}$ is 8000 \mu m/0.18 \mu m. The selected values of $k_1$, $k_2$, $k_3$, and $k_5$ are 4, 4, 12, 10, and 10, respectively. The value of $C_X$ is 5 pF.

The proposed LDO is optimized at $I_{\text{O}} = 50$ mA. In this case, as shown in Fig. 5, the generated zero cancels the dominate pole at 9.44 kHz, and the new dominant pole is at 16.8 kHz. The UGF is, therefore, extended by about two times as compared to LDO without the proposed pole-zero cancellation feature. It is noted that the proposed pole-substitution method is effective when the output current is not very low. In fact, when the output current is very small or zero, the dominant pole is located at ultralow frequency. Original DPFC is dominated, and the created new dominant pole is cancelled by the generated zero. This reveals a fact that the proposed idea is very effective in the moderate-to high-load condition, which is the situation that improvement of load transient response is required.

The simulated loop-gain response of the proposed LDO at $I_{\text{O}} = 0$ A (the minimum), 50 mA, and 100 mA (the maximum) is shown in Fig. 6(a). The achievable UGF at $I_{\text{O}} = 50$ and 100 mA is about 12.5 MHz. The low-frequency loop gain at $I_{\text{O}} = 0$ A is lower than that at $I_{\text{O}} = 100$ mA. This phenomenon is not normal in LDO designs [1], [11]. In order to investigate the reason behind, the operation points of all transistors are carefully investigated. Moreover, a simulation of low-frequency loop gain versus $I_{\text{O}}$ is plotted and shown in Fig. 6(b). It is discovered that the loop gain is reduced when $I_{\text{O}}$ is very low or very high. The reason is that when $I_{\text{O}}$ is very low, the gate voltage of $M_{\text{P}}$ is close to $V_{\text{IN}}$ such that $V_{\text{SD10}}$ in Fig. 2 is small, and hence, the drain resistance of $M_{\text{10}}$ is reduced, causing a drop in the gain of EA. From the simulation data, when $I_{\text{O}} = 0$ A/100 mA, $R_{\text{dm}} = 647 \Omega/9631 \Omega$. When $I_{\text{O}}$ is high, the high drain current of $M_{\text{P}}$ reduces the gain of the power stage. In both cases, the reduction in the gain of EA or $M_{\text{P}}$ decreases the loop gain.

To investigate the stability of the proposed LDO as the location of $z_{\text{ulf}}$ varies, the values of $k_1$, $k_2$, $k_3$, and $k_5$ are altered (refer to (4)) along with a variation of $-20\%$ in the $C_{\text{O}}$ value to shift the dominant pole to a higher frequency so that the UGF is much closer to the parasitic poles. In addition, the ESR is increased by $20\%$ to reduce the ESR zero frequency for more inaccurate pole-zero cancellation. Two extreme cases are considered: 1) 90\% of $k_1$, $k_2$, and $k_3$, and 110\% of $k_5$ to shift $z_{\text{ulf}}$ to a lower frequency, and 2) 110\% of $k_1$, $k_2$, and $k_3$, and
TABLE I
SIMULATED UGF AND PM OF THE PROPOSED LDO WITH \( C_O = 1 \mu F \) AT DIFFERENT ESRs

<table>
<thead>
<tr>
<th>ESR (( \Omega ))</th>
<th>UGF (MHz)</th>
<th>PM (( ^\circ ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>2.46</td>
<td>28.1</td>
</tr>
<tr>
<td>0.05</td>
<td>2.86</td>
<td>27.1</td>
</tr>
<tr>
<td>0.15</td>
<td>5.95</td>
<td>76.5</td>
</tr>
<tr>
<td>0.25</td>
<td>9.40</td>
<td>70.3</td>
</tr>
<tr>
<td>0.35</td>
<td>12.5</td>
<td>63.1</td>
</tr>
<tr>
<td>0.7</td>
<td>20.6</td>
<td>44.3</td>
</tr>
<tr>
<td>1</td>
<td>25.4</td>
<td>34.1</td>
</tr>
</tbody>
</table>

Fig. 7. Simulated loop-gain responses of conventional and proposed LDOs.

90\% of \( k_5 \) to shift \( z_{\text{ulf}} \) to a higher frequency. It should be noted that the \( \pm 10\% \) variations are generally overestimated since vigilant layout design and commercial capacitor with reasonable quality have been ensured. Fig. 6(c) shows the loop-gain simulation curves at \( I_O = 50 \) mA, both with and without variations on \( k_1, k_2, k_3, k_5, C_O \), and ESR, and no significant difference in circuit stability is denoted from the two curves. Also, the phase margins (PMs) of the loop-gains in all cases evaluated are more than 60\( ^\circ \). This proves that the pole-zero cancellation is effective within a decade of frequency.

The selection of the value of ESR has also been investigated and is summarized in Table I. For \( C_O = 1 \mu F \), different ESR values are used to simulate the UGF and PM of the loop-gain response. From the result, the case of ESR of 0.35 \( \Omega \) realizes the best compromise between UGF and PM. Thus, \( C_O = 1 \mu F \) with \( R_E = 0.35 \Omega \) are used in this design.

To demonstrate the improvements achieved by the proposed DPS technique, a conventional LDO (the same circuit structure as in Fig. 3 without the proposed transconductance cell) working in the same supply voltage and output current, as well as connected with the same value of \( C_O \) and ESR is designed and simulated. The simulated results of this conventional LDO and the proposed LDO with DPS are consolidated in Figs. 7 (for frequency responses) and 8 (for load transient responses) for comparison. From Fig. 7, the conventional LDO has loop bandwidth of about 1 MHz and similar PM as the proposed LDO which has loop bandwidth of 12.5 MHz. The selection of \( C_X \) of 5 pF to define the position of the new dominant pole is due to the limitation of the parasitic poles. Load transient responses of both LDO are simulated with \( I_O \) changing from 0 A and 100 mA. Due to the wider loop bandwidth of the proposed LDO, i.e., 12.5 MHz, the response times for rapid increase and decrease of \( I_O \) of the proposed LDO shown in Fig. 8 are about 10 ns, while those of the conventional LDO are 24.2 and 54.87 ns, respectively.

III. EXPERIMENTAL RESULTS

The proposed LDO is implemented in UMC 0.18-\( \mu m \) CMOS technology. Fig. 9 shows the micrograph of the design. The active chip area is 224.9 \( \mu m \times 108.8 \mu m \). The range of \( V_{IN} \), preset value of \( V_O \), maximum \( I_O, C_O \), and its ESR value are exactly the same as the values used in the simulations reported in Section II-D. The measured quiescent current is 135.1 \( \mu A \) when \( V_{IN} = 1.2 \) V. For the performances in the steady state, the measured line regulation is 22.7 mV/V at \( I_O = 100 \) mA, and the measured load regulation is \( -75 \mu V/mA \) at \( V_{IN} = 1.2 \) V. Table II summaries the measured data.
TABLE II
SUMMARY OF PERFORMANCE OF THE PROPOSED LDO

<table>
<thead>
<tr>
<th>Technology</th>
<th>UMC 0.18-μm 1P6M CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage ($V_{IN}$)</td>
<td>1.2–1.8 V</td>
</tr>
<tr>
<td>Preset Output Voltage ($V_O$)</td>
<td>1.0 V</td>
</tr>
<tr>
<td>Output Current ($I_O$)</td>
<td>0–100 mA</td>
</tr>
<tr>
<td>Quiescent Current ($I_Q$)</td>
<td>135.1 μA</td>
</tr>
<tr>
<td>Output Capacitor ($C_O$)/Equivalent Series Resistance ($R_E$)</td>
<td>1 μF/0.35 Ω</td>
</tr>
<tr>
<td>$\Delta V_O/V_O$</td>
<td>2.5%</td>
</tr>
<tr>
<td>Load Regulation ($\Delta V_O/\Delta I_O$)</td>
<td>$-75 \mu V/mA$ at $V_{IN}$ = 1.2 V</td>
</tr>
<tr>
<td>Line Regulation ($\Delta V_O/\Delta V_{IN}$)</td>
<td>22.7 mV/V at $I_O$ = 100 mA</td>
</tr>
<tr>
<td>PSRR</td>
<td>$-35$ dB at 100 kHz $-47$ dB at 3 MHz</td>
</tr>
<tr>
<td>Active Chip Area</td>
<td>224.9 μm x 108.8 μm</td>
</tr>
</tbody>
</table>

Fig. 10. Measured and simulated line transient responses.

For dynamic performances, line and load transient responses as well as PSRR are investigated. Both the measured and simulated line transient responses are shown in Fig. 10. In this investigation, $V_{IN}$ is changed between 1.2 and 1.8 V in 100 ns, where $I_O$ is 100 mA. The selection of an edge time of 100 ns is reasonable since the loop bandwidth is 12.5 MHz and this means the proposed LDO should be able to respond to the line change in 100 ns. From the measured results, the transient error voltage of $V_O$ is within 20 mV. The steady-state error voltage of $V_O$ is 13.6 mV, which yields the previously mentioned line regulation of 22.7 mV/V. On the other hand, the simulated transient and steady-state errors are about 13 and about 10 mV, respectively.

The differences between the measured and simulated results are probably due to the extrapolated values of channel-modulation coefficients of the NMOS and PMOS transistors with nonminimum channel length (noted that the selected channel length of all the NMOS and PMOS transistors used in the EA is 0.5 μm and not the minimum value of 0.18 μm). The inaccurately estimated drain resistance results in the deviation of the loop gain, and hence, the actual loop bandwidth is also slightly different with respect to the estimated expression in (5). As a result, it is possible that the steady-state accuracy (i.e., line regulation) and also dynamic accuracy (i.e., the magnitude of the overshoot in the line transient response) cannot be accurately predicted by simulations. However, the reported measured results are according to the trend predicted by the proposed theory. The steady-state and dynamic performances are shown to be reasonably good.

The measured load transient responses at $V_{IN} = 1.2$ V is given in Fig. 11. Fig. 11(a) indicates clearly the measured load current changing between 0 and 100 mA with edge time of 10 ns. The load transient is generated by connecting a power switch in series with a load resistor. The ON and OFF of the power switching is controlled by an external clock generator. The zoom-in views are provided in Fig. 12(a) and (b). The edge time of $I_O$ change is 10 ns, which is much faster than the
response time of the proposed LDO with a UGF of 12.5 MHz. From the results, the measured undershoot is about 25 mV, and almost no overshoot can be found. In fact, from Fig. 12(a), the undershoot of $V_O$ occurs within 10 ns. This undershoot should not be coming from the LDO’s response since the response time of LDO is about 100 ns (i.e., $\text{UGF} = 12.5 \text{MHz}$). The cause of this rapid undershoot is probably due to the bond-wire inductance and/or the inductance of the output capacitor. As a result, the true undershoot of $V_O$ should be counted at around 100 ns after the load change. Thus, the true undershoot is less than 20 mV. The calculated transient error voltage, which is a product of the change of $I_O$ and the ESR value, is 35 mV.

Similar to the line transient responses, the simulated results cannot estimate the transient overshoot and load regulation accurately. But, the measured results show much better performance than the simulated one. Finally, a careful investigation of the overshoot observed in the simulation when $I_O$ decreases from 100 mA to 0 A is conducted. As a remark, this overshoot does not appear in measurement.

Fig. 13 shows the measured PSRR of the proposed LDO at $V_{IN} = 1.2 \text{V}$ and under $I_O = 100 \text{mA}$, which is the worst case since the drain resistance of $M_P$ would be the smallest with minimum $V_{SD}$ and maximum $I_{SD}$. As such, the isolation ability between $V_{IN}$ and $V_O$ by $M_P$ alone should be the worst. The PSRR in this situation relies on the loop gain and also its loop bandwidth to correct the high-frequency error voltages at $V_O$. In particular, the measured PSRR values at 100 kHz and 3 MHz are $-35$ and $-47 \text{ dB}$, respectively. Again, the measured results show a similar trend as the simulations do. The difference may be mainly due to the inaccurate simulation model of the channel-modulation effect to cause the difference of the PSRR in the low- and mid-frequency range. For the high-frequency response, it may be due to the influence of the inductance of the output capacitor.

A PSRR dip is noted at around 2.5 MHz in the simulated curve shown in Fig. 13. An analysis is conducted and it is found that having less bias current in the proposed transconductance cell and a capacitor with a smaller ESR can enhance the PSRR in the range of 1 to 4 MHz. With less bias current in the proposed transconductance cell, the equivalent resistance between the supply and the cell increases. Furthermore, a smaller ESR implies that the output capacitor is more ac short-circuited between the LDO output and the clean ground. The lowering of both bias current and capacitor ESR can improve the PSRR in the moderate-frequency range (i.e., 1–4 MHz).

Finally, the proposed LDO is compared against the state-of-the-art designs implemented in technologies with similar feature size so that the power consumption, response speed, as well as transientundershoots and overshoots do not take the advantage of the small parasitic capacitances of the advanced technologies. Two state-of-the-art designs reported in [17] and [18] are chosen for comparison. A design based on zero-generation for pole-zero cancellation [3] is also included in the benchmarking though the design is based on 0.5-$\mu$m CMOS process. Table III shows a summary of the comparison.

Although the proposed LDO consumes more quiescent current due to the proposed transconductance cell, it outperformed the other three LDOs in terms of load regulation (related to steady-state accuracy) and the magnitude of undershoot/overshoot (related to transient speed and accuracy). It is noted that the maximum load current for the design in [18] is only 25 mA. Theoretically, the overshoot and undershoot should be increased by four times (which are 40 mV for undershoot and 60 mV for overshoot, respectively) if the same circuit is
revised to deliver 100 mA, which is the same output-current level of the proposed LDO.

IV. CONCLUSION

A CMOS LDO with DPS has been reported in this paper. The DPS is based on a triple-input EA which generates a 90° phase leading signal to drive the power transistor such that the overall delay of the signal path can be reduced. The principle of operation of the proposed LDO design and experimental results has verified that the proposed idea is able to improve the dynamic performances of LDO substantially. The potential drawback of the proposed DPS technique is that the quiescent current of the LDO is higher, but it can be reduced when the transconductance of the input differential pair is reduced. However, the achieved current efficiency remains high and equals to 99.86%.

REFERENCES


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