A Robust Cross-Regulation-Suppressed Single-Inductor Multiple-Output DC-DC Converter with Duty-Regulated Comparator Control

Yanqi Zheng*, Marco Ho*, Ka Nang Leung*, Jianping Guo†‡ and Hua Chen*
Email: {yqzheng, mho, knleung}@ee.cuhk.edu.hk guojp3@mail.sysu.edu.cn
*Department of Electronic Engineering, The Chinese University of Hong Kong, Hong Kong SAR, China
†School of Physics and Engineering, Sun Yat-sen University, Guangzhou, China
‡SYSU-CMU Shunde International Joint Research Institute, Foshan, China
#Department of Electrical, Computer and Energy Engineering, University of Colorado Boulder, Boulder, Colorado, 80309

Abstract—A robust cross-regulation-suppressed single-inductor multiple-output (SIMO) dc-dc converter with duty-regulated comparator control is proposed. The control scheme effectively combines comparator-based and linear-compensator-based controllers to achieve fast load-transient response and low cross regulation to other output channels simultaneously. The control algorithm does not rely on duty-inductor-current feed-forward which is sensitive to the accuracy of inductor-current sensor. As a result, it can provide robust cross-regulation suppression for a wide range of loading for the SIMO dc-dc converter. Moreover, together with the average-inductor-current control, the proposed control algorithm is suitable for SIMO dc-dc converter which has auto-buck-boost property for each sub-converter, which makes the SIMO converter suitable for dynamic voltage scaling applications.

Keywords— Auto buck-boost, comparator based, current mode, cross regulation, single-inductor multiple-output dc-dc converter.

I. INTRODUCTION

Single-inductor multiple-output (SIMO) dc-dc converter is a potential solution for applications requiring multiple supplies where the output voltages and power for each supply are largely different [1]. In the past decade, some works were reported to solve different problems and to improve the various performances of a SIMO dc-dc converter [1]–[9]. To alleviate the limitation of output power in the discontinuous conduction mode (DCM) operation, pseudo-DCM and freewheeling feedback technique were proposed [1], [2]. To reduce cross regulation (CR), charge balanced method [3], [4], time-limited power distribution [5], and small-signal parameter fitting [9] were reported. To improve the transient speed, comparator-based control algorithm has been adopted [6], [7]. To enable dynamic voltage scaling (DVS) for SIMO dc-dc converter, buck-boost technique is used [8]. By considering the differences of the inductor current during operation, SIMO dc-dc converters are usually classified into two types: time-multiplexing control (TMC) and ordered power-distributive control (OPDC). There are tradeoffs between power efficiency and cross regulation. With different voltage controllers, SIMO dc-dc converter can also be sorted into compensator-based and comparator-based controls. Similar to the single-output dc-dc converter, compensator-based control has lower transient speed while comparator-based one suffers from switching noise and voltage ripples.

In this paper, a SIMO dc-dc converter with proposed duty-regulated comparator control (DRCC), which effectively combines both the comparator-based and linear-compensator-based controllers, is developed. With the proposed DRCC method, not only cross regulation is suppressed, but the design is also independent of both the accuracy of current sensor and loading condition of each channel. Moreover, there is no operation-frequency variation as in the comparator-based controller. Hence, no phase-locked loop circuit is required.

II. CROSS REGULATION IN SIMO DC-DC CONVERTER

Cross regulation is a special issue in SIMO dc-dc converter design. The origin of this problem can be described using Fig. 1, which shows the inductor current ($i_L$) of a single-inductor dual-output (SIDO) dc-dc converter. After a step of load change is applied to Channel 1, the duty cycle for each channel will be re-arranged. The criterion for no cross regulation to Channel 2 is that $i_{L,(1)}(1) \cdot D_{2(1)} = i_{L,(n)}(n) \cdot D_{2(n)}$, provided that inductor current ripple is ignorable; otherwise, CR appears and Channel 2 contains undershoots or overshoots. This can be eliminated by duty-inductor-current feed-forward such as charge balance [3], [4]. It can be observed that the duty cycle of a channel can be expressed as

$$\frac{D}{D} \approx \frac{i_s}{i_{L,d}}$$
where $D$ is the duty cycle, $i_c$ is the control signal, $T_S$ is the switching period, and $i_{LA}$ is the average inductor current. As a result, the output current of a channel can be set to a constant:

$$i_c = Di_{LA} = i_s = \text{const.} \quad (2).$$

However, it is only valid when the current sensor provides an accurate value of the true inductor current. If there is a dc offset of $I_{OS}$ at the current sensor, the average inductor current becomes $i_{LA} + I_{OS}$ which makes the output current becomes

$$i_c = D(i_{LA} + I_{OS}) = i_{LA} + I_{OS} \neq \text{const.} \quad (3).$$

The extra part of the output current contributes to the CR during load transient. Since there is no a design freedom for the duty cycle of the last channel in fixed-frequency designs, the last channel suffers from the summation of all mismatches generated in the previous channels. In addition to the these problems, the inductor current changes according to the performance of reference tracking to its control signals. If an inductor-current controller is of narrow bandwidth, CR will also be introduced during load transient.

Another solution to attenuate CR is to use comparators to regulate output voltages [6], [7], which does not depend on duty-inductor-current feed-forward. However, in addition to the common problems in comparator-based design, this method suffers from two extra problems. First, although comparators provide high-speed responses, they behave invariably to both transient and idle channels. As a result, the sudden enlargement to the duty period of the transient channel will be equivalent to decrease of the operation frequency of the idle channel. The equivalent ripple appears to be comparable to the CR effect. Second, if the SIMO dc-dc converter consists of boost sub-converter, or even a sub-converter with output voltage slightly smaller than the input voltage, the enlargement of the duty cycle does not guarantee the increase of the inductor current. This is similar to the situation of a single-channel boost converter. The period increase that is used to charge the output capacitor cannot provide an essentially larger current to the output due to the corresponding decrease of the inductor current (which can also be modeled as a right-half-plane zero). CR effect may be worse, and the system may even be unstable. In summary, the existing methods are not all suitable for SIMO dc-dc converter with auto buck-boost property.

III. PROPOSED DUTY-REGULATED COMPARATOR CONTROL

A. Components and Signal Generations of DRCC

To solve the aforementioned problems, a duty-regulated comparator control (DRCC) method is proposed. To demonstrate its operations, a SIDO dc-dc converter has been designed and its control diagram is shown in Fig. 2. It can be seen that the MOSFET switches in the power stage (top part of Fig. 2) are controlled by four digital signals, $D_f$, $D_r$, $D_i$, and $D_s$, by the control logic block (centre of Fig. 2). $D_i$ and $D_s$ are pulse-width modulation (PWM) signals that control the current to be delivered to Channel 1 or 2, respectively. $D_r$ controls the rising of the inductor current by controlling SW_PI and SW_NO, so that sufficient current is charged to the inductor from the voltage source. Conversely, $D_f$ controls the falling of inductor current, by connecting the inductor to the input source via SW_PI, or to the ground via SW_NI. $D_f$ and $D_r$ are actually generated by the inductor current controller, where essentially consists of a PI controller, $C(s)$, that controls the inductor current $i_L$. The signals $v_i$ and $v_f$ reflect the values in which $i_L$ has to be decreased or increased, respectively. Combining with the ramp signal, the PWM signals of $D_r$ and $D_f$ are generated. Note that $D_f$ and $D_r$ cannot be larger than zero at the same time. This operation guarantees a low average inductor current of the SIMO converter no matter it is boost-dominated or buck-dominated, which reduces the conduction loss so that high efficiency can be achieved.

In fact, the duty cycles ($D_{ij}$, where $i$ is channel number) are generated by the minimum pulse width of the outputs of two duty-cycle generators—$D_{ui}$ from linear-compensator-based generator, and $D_v$ from comparator-based generator. The linear-compensator-based duty-cycle generator takes inputs from the charge-pump-based (CP-based) integrator, $v_{ui}$, and the ramp generator, $v_r$. The ramp generator functions similarly as in conventional voltage mode dc-dc converters, where the CP-based integrator acts as a first-order linear compensator, which would be described later. On the other hand, the comparator-based duty-cycle generator receives inputs from error voltages of the channels, $v_{ui}$, and the ramp signals from the ripple-compensation ramp generator, $v_{ri}$. The error voltages are simply the differences between targeted and actual output voltages for each channel. The ripple-compensation ramp generator not only attenuates the sensitivity of the comparator to the output ripple of the converter [2], it is also used to generate the comparator-based duty cycle even output PMOS is off. Moreover, the outputs of the linear-compensator-based duty-cycle generator will try to follow the outputs of the comparator-based generator as controlled by the CP-based integrator. The duty cycle difference is defined as $\Delta D_i = D_{ui} - D_{ui'}$. When $\Delta D_i > 0$, which means $D_u$ has a longer pulse than $D_{ui'}$, the charge pump will increase $v_{ui}$ via the upper current source. As a result, $D_{ui}$ will increase until the pulse widths of
$D_{a}$ and $D_{c}$ are equal. Similarly, if $\Delta D_{i} < 0$, via will be reduced by the lower current source in the CP-based integrator, so that $D_{ia}$ will be shortened until it has the same pulse width as $D_{ic}$.

Once the duty cycles (i.e. $D_{1}$ and $D_{2}$) are computed, the total desired period, which consists of $D_{a}$ and $\sum D_{ia}$ can be determined. However, if $T_{wa} = D_{a} + \sum D_{ia} > 1$, it means that the total desired duty period is longer than the operation period of the SIMO dc-dc converter. If $T_{wa} < 1$, it means that the desired period is shorter than the operation period, in which an idle period of inductor current will be inserted.

**B. Operation Principles for Cross-Regulation Suppression**

The operation principles of the proposed method can be explained when a load transient is applied to one of the output channels of the converter. For instance, consider when the output current of Channel 1 (i.e. $i_{o1}$) is suddenly reduced, as shown in Fig. 3(a). The high-speed comparator can provide immediate decision when the output voltage exceeds the reference voltage. As a result, the duty cycle generated by the comparator (i.e. $D_{ic}$) will be reduced accordingly in a short period of time in respond to the high-to-low current change of Channel 1. Since now the compensator-based duty cycle, $D_{ia}$, is shorter in duration than $D_{ic}$, it will be reduced gradually to follow $D_{ic}$. Simultaneously, $D_{oa}$ increases slightly since an internal feedback will try to make $D_{a} + \sum D_{ia} = 1$. The total desired period is now shorter than operation period (i.e. $T_{wa} - 1 < 0$), and idle period is enforced. Therefore, inductor current will be decreased. Responding to the reduced $i_{i}$ (only described with its average value in the Fig. 3), the duty cycle of another channel (both $D_{oa}$ and $D_{oa}$) will be increased in order to provide constant output current, and the temporary idle period is eliminated in due course. Since the inductor current is reduced slowly compared to the comparator response, the cross regulation caused by current feed-forward is ignorable.

If the load current of Channel 1 is increased, as shown in Fig. 3(b), the comparator will try to increase the duty cycle of the sub-converter. However, the output of the compensator (i.e. $D_{oa}$), which reflects the original loading condition, will limit the duty cycle due to the dominance of the minimum duty cycle. The difference between $D_{ia}$ and $D_{ic}$ will be captured by the CP-based integrator, which will prepare the charging of val1. However, since there is no idle period for the inductor current, there is no room for the duty cycle of Channel 1 to be increased. $T_{wa} - 1 > 0$ and overflow is signaled. As a result, the pull-up current source of the charge pump is disabled, and $v_{o1}$ cannot be increased. This operation prevents the CR originated from any sudden increase of the duty cycle of the active channel, as it happens with the conventional comparator-based controller. On the other hand, inductor current will be boosted by the inductor-current controller in respond to the summation of error voltages and the integration of magnitude of duty-period overflow (i.e. $T_{wa} - 1$). Then, the duty cycle of Channel 2 will decrease in order to keep its output current constant. As before, the comparator-based control is able to guarantee superb regulation to prevent voltage shooting, so that CR caused by the increase of $i_{i}$ can be eliminated. The reduction of $D_{oa}$ will cause the reduction of $D_{oa}$ as well as the decrease of $i_{oa}$. Thus, $T_{wa} - 1 < 0$ and overflow no longer occurs. The pull-up current source of the charge pump is re-enabled, and $D_{oa}$ is now free to be increased. Finally, the duty cycles of each channel are redistributed and the system is stabilized.

**C. Implementation of Comparator-Based Duty Generator**

It is noted that the comparator-based control cannot guarantee to generate a duty period that is smaller than the operation period. As a result, an interleaving technique of phase signals is applied to generate targeted duty cycles across operation periods. The resultant implementation of the duty generator is shown in Fig. 4. The waveforms demonstrate an instantaneous period when $D_{ic} > D_{ia}$. Pulse $en\_vr1$ appears soon after charging period (controlled by $D_{ic}$) is completed. It generates $ph1a$ and $ph1b$, two out-of-phase signals that are half of the operation frequency, take turns to generate control signals which sample the error voltage, $v_{ci}$, and generate the compensation ramps. This guarantees $D_{ia}$ or $D_{oa}$ can be captured by the phase detector (PD) even when the output PMOS is off. Note that the actual duty cycle of Channel 1 is limited by $D_{ic}$ due to the minimum duty-cycle rule. Detailed analysis is omitted due to space limitation.

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**IV. SIMULATION RESULTS**

In order to verify the DRCC method, an auto-buck-boost SIDO converter is modelled in Simulink. The simulation parameters are shown as follows: $V_{G} = 3V$, $V_{o1} = 1.8V$, $V_{o2} = 5V$, $L_{1} = 4.7\mu H$, $R_{ESR,L1} = 150m\Omega$; $C_{1} = C_{2} = 10uF$, $R_{ESR,C1} = R_{ESR,C2} = 20m\Omega$, $f_{s} = 1MHz$. For comparison, a converter with duty-inductor-current feed-forward has also been modelled, and its simulation results are shown in Fig. 5. It can be seen that with perfectly accurate current sensor, the CR (in red circles) is not very severe during a 400-mA of load transient. However, with only a 200-mA offset of inductor current, considerable CR has been generated. This demonstrates the rigidity of the duty-inductor-current feed-forward method.
On the other hand, the simulation results prove that the proposed DRCC can effectively suppress CR (in red circles) in different output and loading conditions. Fig. 6 shows the results when the boost channel is undergoing a 400-mA load transient, while the buck channel is with heavy and light loads. Fig. 7 shows the load transients that take place in the buck channel, with heavy and light loading is drawn from the boost channel. The CR suppressions in all different cases show the robustness of the DRCC method, which is independent of accuracy of current sensor and RHP-zero effect in boost converter. The steady state waveform of inductor current shown in Fig. 8 also demonstrates the auto-buck-boost ability. Performance comparisons with other state-of-art designs are shown in Table I. It can be seen that it has the best cross-regulation performances.

### Table I. Performance Comparisons with Other SIMO Designs

<table>
<thead>
<tr>
<th>Type</th>
<th>Auto Buck-Boost</th>
<th>Switching Frequency (MHz)</th>
<th>Inductor (µH)</th>
<th>Capacitor (µF)</th>
<th>Self Regulation @ transient (mV/mA)</th>
<th>Cross Regulation @ transient (mV/mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>Boost NO</td>
<td>1</td>
<td>1</td>
<td>33</td>
<td>1</td>
<td>0.2</td>
</tr>
<tr>
<td>[3]</td>
<td>Buck NO</td>
<td>1.2</td>
<td>2.2</td>
<td>4.7</td>
<td>0.6</td>
<td>0.067</td>
</tr>
<tr>
<td>[4]</td>
<td>Boost NO DCM</td>
<td>1</td>
<td>9.4</td>
<td>0.67</td>
<td>0.03</td>
<td></td>
</tr>
<tr>
<td>[6]</td>
<td>Buck NO</td>
<td>2</td>
<td>4.7</td>
<td>10</td>
<td>0.93</td>
<td>0.31</td>
</tr>
<tr>
<td>[7]</td>
<td>Buck NO</td>
<td>4.7</td>
<td>10</td>
<td>0.16</td>
<td>0.04</td>
<td></td>
</tr>
<tr>
<td>[8]</td>
<td>Buck-Boost YES</td>
<td>2</td>
<td>2.2</td>
<td>20</td>
<td>0.92</td>
<td>0.02</td>
</tr>
<tr>
<td>This work</td>
<td>Buck-Boost YES</td>
<td>1</td>
<td>4.7</td>
<td>10</td>
<td>&lt;0.5</td>
<td>&lt;0.02</td>
</tr>
</tbody>
</table>

### V. CONCLUSIONS

A novel duty-regulated comparator control (DRCC) SIMO auto-buck-boost dc-dc converter has been proposed in this paper. The design can provide robust cross-regulation (CR) suppression for a wide range of loading combinations of sub-converters. Detailed explanations have been given to show that both fast load-transient responses and small CR can be attained. Simulation results have been shown to prove the idea.

### REFERENCES


