A 124-dB Double-Gain-Boosted Cascode Amplifier with 92% Rail-to-Rail Output Swing

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Abstract—A CMOS amplifier with 124-dB dc gain and 92% rail-to-rail output swing is proposed in this paper. The proposed amplifier uses double gain-boosting technique, enabling triode-region operation in cascode output stage. The design is fabricated in a commercial 0.35-μm CMOS technology. The active chip area is 84 μm × 170 μm. Experimental results show that with the supplies of ±1 V, the high-gain region is extended beyond −0.93 V and 0.91 V. The unity-gain frequency is about 300 kHz with a phase margin of 65° when driving a loading capacitor of 100 pF. Signal distortion is significant reduced compared to the conventional design due to extension of the high-gain region in the proposed amplifier.

I. INTRODUCTION

High-gain wide-swing amplifiers are always in high demand in different analogue circuit designs. By applying a predefined feedback network, the closed-loop gain can be properly controlled as long as the open-loop gain of the amplifier is high. The relationship is given by

\[
A_C = \frac{\frac{A_O}{f}}{1 + A_O f} \approx \frac{1}{f}
\]  

(1)

where \(A_C\) and \(A_O\) are the closed-loop gain and open-loop gain of the amplifier, respectively, and \(f\) is the feedback factor. However, the open-loop gain is significantly reduced when \(V_o\) is close to the supply rails due to the reduction of the output resistance in these regions. As a result, the closed-loop gain is significantly degraded near supply boundaries, and distortion due to finite gain error becomes more prominent.

Traditional, cascode structure is used to boost the voltage gain of an amplifier by increasing the output resistance by a factor of \(g_{mro}\) [1]–[8]. Nevertheless, the vertically built structure reduces output swing significantly, and hence wide-swing cascode and other circuit structures have been proposed [4]–[8]. Although design of cascode amplifier using transistors operating in triode region has been reported to relax the constraints of the output swing [8], the enhancement of the output resistance is sacrificed when compared to the normal cascode structure. Obviously, it would be advantageous to extend the output headroom and to increase the output resistance simultaneously.

In this paper, a double-gain-boosted ultrawide-swing amplifier is proposed and analyzed. A double-gain boosting cascode structure will first be presented and analyzed. Simulation results will be discussed next. Finally, experimental results will be reported and conclusion will be given.

II. DESIGN OF CASCODE AMPLIFIER WITH DOUBLE GAIN-BOOSTING

Conventionally, cascode output stage has been used in amplifiers to greatly increase the output resistance, thus enhancing the open-loop gain. To further increase the output resistance, one of the well known techniques is gain boosting [1], [2]. The proposed amplifier that employs this technique recursively—the gain-boosting amplifier is in turn being gain-boosted—is shown in Fig. 1(a). It consists of a conventional current-mirror amplifier with gain-boosted cascode output. The upper branch of the cascode structure is gain-boosted by an auxiliary amplifier \(A_{UPPER}\), where the lower branch is gain-boosted by another auxiliary amplifier \(A_{LOWER}\). The auxiliary amplifiers, shown in Fig. 1(b) and (c), are in turn current-mirror amplifiers with gain-boosted cascode output. It is noteworthy that \(M_{A5}, M_{A6}, M_{A9}\) and \(MA10\) are designed to operate in triode-region, thus extending the output swing range.

At the lower branch of the main amplifier, \(V_{DS46}\) is determined by the value of \(V_2\), which is regulated to be equal to \(V_1\) by \(A_{LOWER}\). \(V_1\) is generated by a self-cascode structure formed by \(M_{A5}\) and \(M_{A7}\) [9]. Therefore, \(V_{DS45}\) is given by

\[
V_{DS45} = V_1 - V_{SS} = V_{GS45} - V_{GS47} - V_{SS}
\]  

(2)

Theoretically, when the size of \(M_{A7}\) is greater than four times that of \(M_{A5}, M_{A5}\) will operate in the saturation region [2], [9]. In order to guarantee \(M_{A5}\) operate in the triode region, \(M_{A7}:M_{A5} = 2:1\) is chosen in the design. It is noted that when the size of \(M_{A7}\) is getting closer to that of \(M_{A5}, V_{DS45}\) becomes smaller and \(M_{A5}\) is pushed deeper into the triode region. On the other hand, \(A_{LOWER}\) makes \(V_{DS46}\) very close to \(V_{DS45}\). Moreover, since \(V_3\) at the output of \(A_{LOWER}\) is a fixed voltage, dynamics is not required to be considered when designing \(A_{LOWER}\). As a result, \(A_{LOWER}\) is composed of a typical gain-boosting structure. \(M_{L3}\) forms a single-transistor auxiliary amplifier to detect the drain voltage of \(M_{L6}\), then to provide the control voltage to the gate of \(M_{L7}\). Similarly \(M_{L11}–M_{L13}\) provide the gain-boosting at

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the upper branch of ALOWER. Since the output dynamics is not a concern in ALOWER, M_{A6}–M_{A8} and M_{L11}–M_{L13} are designed to operate in saturation region, to generate very large output resistance, hence very high gain to ALOWER. This is used to compensate the drain-resistance reduction due to the triode-region operated M_{A6}.

\[ P_{L12} = \frac{1}{(r_{ds12} // r_{ds4})C_{GL3}} \]  

\[ P_{\text{LOWER}} = \frac{1}{\left[ r_{ds6} \left( \frac{g_{mL5} r_{ds6}}{g_{mL5} r_{ds6} // r_{ds6}} \right) \right] C_{GL3}} = \frac{1}{R_{\text{LOWER}} C_2} \]  

where \( P_{L12} \) and \( P_{\text{LOWER}} \) are the poles at the drain of M_{A6}, the drain of M_{L12}, and the output of ALOWER. \( g_{mL7} \) and \( r_{ds8} \) is the transconductance and drain resistance of the substrate transistor M_{l}, respectively. For example, \( g_{mL7} \) is the transconductance of transistor M_{L7}, and \( r_{ds8} \) is the drain resistance of transistor M_{L8}. \( C_{GL3} \) and \( C_{GL13} \) are the lumped parasitic capacitances appeared at the gates of M_{L7} and M_{L13}, respectively. \( C_2 \) is the capacitor at the output of ALOWER, and \( R_{\text{LOWER}} \) is the equivalent output resistance of ALOWER. Generally, the output resistance of the gain-booster stage is drastically increased. Therefore, the product of such output resistance with a capacitor would be much larger than the \( RC \)-product of the simple single-transistor gain-booster stage, so that \( P_{L12} \) and \( P_{\text{LOWER}} \) are located at much higher frequency than \( P_{L12} \). Then, the transfer function of ALOWER can be approximated as

\[ A_{\text{LOWER}}(s) \approx \frac{g_{mL1} R_{\text{LOWER}}}{s + \frac{1}{R_{\text{LOWER}} C_2}} \]  

Similarly, the transfer function of AUPPER is given as

\[ A_{\text{UPPER}}(s) \approx \frac{g_{mU1} R_{\text{UPPER}}}{s + \frac{1}{R_{\text{UPPER}} C_1}} \]  

where \( g_{mU1} \) is the transconductance of M_{U1}, \( R_{\text{UPPER}} \) is the equivalent output resistance of AUPPER, and \( C_1 \) is the capacitor at the output of AUPPER. Again, since the double gain-boosted main amplifier has significant enhanced gain with respect to the gain-booster auxiliary amplifiers, the proposed amplifier is a single-pole system. The transfer function is given by

\[ A(s) \approx \frac{g_{mL1} \left( r_{ds6} g_{mL5} r_{ds6} // r_{ds6} g_{mL5} / r_{ds6} \right) R_{\text{LOWER}}}{s + \frac{1}{\left( r_{ds6} g_{mL5} r_{ds6} // r_{ds6} g_{mL5} / r_{ds6} \right) C_{GL3}}} \]  

The reduction of \( r_{ds6} \) and \( r_{ds10} \) due to triode-region operated M_{A6} and M_{A10} are compensated by the proposed double gain-booster, while the system is maintained to be single-poled. In fact, nested structures of gain-booster can be proven to perform as single stage amplifier once the condition criteria are met. Detailed analysis is omitted here due to limited pagination.

III. SIMULATION RESULTS OF PROPOSED AND CONVENTIONAL AMPLIFIERS

In order to demonstrate the improvement of the proposed design, a simple current-mirror amplifier is designed for comparison. Transistor sizes and biased conditions are the same. The conventional amplifier only differs from the proposed amplifier that the conventional one has no cascode.
structures and no gain-boosting amplifiers. Open-loop and closed-loop dc transfer characteristics of both amplifiers are simulated using a commercial 0.35-\(\mu\)m technology. The ideal closed-loop gain is designed to be –10 V/V. The simulation results of the proposed amplifier (solid line) and of the conventional design (dashed line) are shown in Fig. 2. The open-loop gains of the proposed amplifier at 0.908 V, 0 V and –0.936 V are 62 dB, 124 dB and 90 dB, respectively. Although the open-loop gain is constant over the input range, the significant gain improvement makes sure the closed-loop gain is steadily maintained at wide range of output. Furthermore, the high-gain region is significantly extended due to the triode-region operated transistors.

Fig. 2. Simulated dc open-loop and closed-loop transfer characteristics of proposed amplifier (solid lines) and conventional amplifier (dashed lines).

IV. EXPERIMENTAL RESULTS

Both the proposed and the conventional amplifiers are fabricated using AMS 0.35-\(\mu\)m CMOS process. The threshold voltages for NMOS and PMOS devices are about 0.5 V and -0.65 V, respectively. The active area of the proposed amplifier is 84 \(\mu\)m \(\times\) 170 \(\mu\)m, and the chip micrograph is shown in Fig. 3. Both amplifiers operate under supplies of ±1 V. The measured current consumptions of the proposed and conventional amplifiers are 99 \(\mu\)A and 75 \(\mu\)A, respectively. Both amplifiers are set up with inverting configuration and ideal closed-loop gain of -10 V/V. An output capacitor of 100 pF is connected to the output of each amplifier. Table I shows the summary of the measured performances.

![Chip micrograph of the proposed amplifier.](image)

<table>
<thead>
<tr>
<th>Technology</th>
<th>Proposed</th>
<th>Conventional</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages</td>
<td>±1 V</td>
<td>±1 V</td>
</tr>
<tr>
<td>Output Capacitor</td>
<td>99 (\mu)A</td>
<td>75 (\mu)A</td>
</tr>
<tr>
<td>Simulated Maximum Open-Loop Gain</td>
<td>1.57 MV/V (124 dB)</td>
<td>463 V/V (53 dB)</td>
</tr>
<tr>
<td>Unity-Gain Frequency</td>
<td>300 kHz</td>
<td>300 kHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>65°</td>
<td>68.5°</td>
</tr>
<tr>
<td>Output Swing</td>
<td>-0.93 V &lt; (V_O) &lt; 0.91 V (92% rail-to-rail)</td>
<td>-0.86 V &lt; (V_O) &lt; 0.81 V (83.5% rail-to-rail)</td>
</tr>
</tbody>
</table>

Fig. 4 shows the measured closed-loop frequency responses of both amplifiers. The input dc voltage is at the middle of the supplies (i.e. \(V_IN = 0\) V). Both amplifiers have the same unity-gain frequency (UGF) and nearly identical phase margins (PMs). This proves that the proposed double gain-boosting structure does not affect the frequency response when the gain-boosting poles are at much higher frequencies than the gain-boosted poles. The phase margins of both the proposed and conventional amplifiers are less than the theoretical value of a single-pole system (i.e. PM = 90°). These are due to the parasitic capacitance of the current mirrors under low-power condition, introducing some parasitic poles close to the UGF. The proposed design has 3.5° PM less than the conventional one because the self-cascode structure has slightly larger parasitic capacitances, but the effect does not cause impact to the stability of the proposed amplifier. The low-frequency closed-loop gain of the conventional amplifier deviates from the ideal –10 V/V due to finite gain error since it has smaller gain. The proposed design has a better close-loop gain performance.

![Measured closed-loop frequency responses of proposed amplifier (solid lines) and conventional amplifier (dashed lines).](image)
With reference to the frequency responses in Fig. 4, the phase delay of both amplifiers is negligible when input signal frequency is less than 1 kHz. As a result, a 400-Hz 300-mVpp sinusoidal signal is input to both proposed and conventional amplifiers, and the dc transfer characteristics are measured and shown in Fig. 5. The x-axis and y-axis represent $V_{IN}$ and $V_O$, respectively. The proposed design achieves linear amplification of -10 V/V when $V_O$ is ranged between -0.93 V to 0.91 V. On contrast, the output swing of the conventional design is vaguer due to the smaller open-loop gain.

![Fig. 5. Measured closed-loop dc transfer characteristics of (a) proposed amplifier and (b) conventional amplifier.](image)

The same input signal (400-Hz 300-mVpp) is applied to both amplifiers when the transient responses are investigated. Since the supply voltage are ±1 V, the ideal -10-V/V amplification of the closed-loop configuration will generate clipped-off outputs. The measurement results are shown in Figs. 6 and 7. Note that the input signals have been inverted to be better compared with the output signals. It can be seen that in the proposed design, the output waveform follows the input more closely and to a wider range, which is due to the extended high-gain region to 92% of the supply rails.

![Fig. 6. Measured clipping transient response of proposed amplifier.](image)

![Fig. 7. Measured clipping transient response of conventional amplifier.](image)

**V. CONCLUSION**

An amplifier with double gain-boosting technique is presented in this paper. The proposed design achieves 124-dB dc gain and an output swing of 92% of the supply rails. The overall amplifier can be regarded as a single-pole system since the poles of the auxiliary amplifiers locate at much higher frequency than the gain-boosted amplifier. By using triode-region operating transistors, the output swing is significantly improved. As a result, the drastically increase of output resistances and extension of the high-gain region are achieved simultaneously. Experimental results verify the improvements of the proposed amplifier in distortion and output swing, without sacrificing bandwidth or stability. In fact, according to the theoretical analysis, nested gain-boosting can be further applied to an amplifier while maintaining the advantages of single-pole system, once proper condition criteria are made.

**REFERENCES**


