An Area-Efficient 96.5%-Peak-Efficiency Cross-Coupled Voltage Doubler With Minimum Supply of 0.8 V

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Abstract—An area-efficient cross-coupled voltage doubler (CCVD) with no reversion loss using first-level gate-control mechanism is presented. The proposed design does not require area-consuming resistors or extra power MOSFETs to prevent reversion currents. Through the first-level gate controls, the proposed CCVD is able to use internal nodes to drive the gates of the power MOSFETs without extra buffers, thus further reducing the silicon area and power consumption. The proposed design has been fabricated in a commercial 0.35-μm CMOS technology ($V_{THN} \approx 0.59$ V, $V_{THP} \approx -0.72$ V), with an active area of only 0.49 mm$^2$. Experimental results show that it can achieve a maximum of 96.5% power efficiency value under a supply voltage range of 0.8–1.6 V with a maximum loading current of 30 mA.

Index Terms—Charge pump, cross-coupled voltage doubler (CCVD), first-level gate control, reversion loss, voltage doubler.

I. INTRODUCTION

The cross-coupled voltage doubler (CCVD) is a type of switched-capacitor dc–dc converter in which the output voltage is about twice of the input voltage. Compared with a conventional charge pump, CCVD can reduce either the output voltage ripple or the output capacitance by half, with the same input switching frequency [1]. However, the power efficiency of CCVD can be severely reduced by reversion loss, which is caused by pumped charges flowing from high-voltage nodes back to low-voltage nodes.

Several approaches have been proposed by researchers to tackle the issue [1]–[4]. $RC$ delay is used in [1] to make sure that the MOSFETs are shut off faster than they are turned on. However, area-consuming polyresistors have been used since the required resistances have to be very accurate to control the switch-on times. In [2], two identical CCVDs with opposite phases working in parallel have been presented to prevent reversion loss. Hence, the silicon area occupied as well as the number of flying capacitors would be doubled. To reduce the chip area and to eliminate reversion loss simultaneously, level shifters are used to switch off the output PMOSFETs in [3]. However, since the level shifters and their buffers draw power from the output of CCVD itself, the power MOSFETs have to be designed with greater size. As a result, the chip area cannot be minimized and switching loss would also be increased. Additional blocking power MOSFETs have been suggested to eliminate the reversion loss [4], but the additional chip area for extra power MOSFETs and their control circuity, as well as additional capacitors, are steep prices to be paid.

In this brief, a simple and effective gate-control mechanism is proposed to eliminate reversion loss in CCVD. First-level gate controls [5] are adopted to properly isolate the charged capacitors in the dead-time period to prevent reversion currents. No level shifters or extra buffers are required; hence, the chip area and switching loss would be similar to those of the conventional CCVD, whereas the efficiency is improved significantly.

II. REVERSION LOSS IN CONVENTIONAL CCVD

A. CCVD Operations

The schematics of a conventional CCVD are shown in Fig. 1. The bulks of all PMOSFETs are connected to their sources, and the required resistances have to be very accurate to control the switch-on times. In [2], two identical CCVDs with opposite phases working in parallel have been presented to prevent reversion loss. Hence, the silicon area occupied as well as the number of flying capacitors would be doubled. To reduce the chip area and to eliminate reversion loss simultaneously, level shifters are used to switch off the output PMOSFETs in [3]. However, since the level shifters and their buffers draw power from the output of CCVD itself, the power MOSFETs have to be designed with greater size. As a result, the chip area cannot be minimized and switching loss would also be increased. Additional blocking power MOSFETs have been suggested to eliminate the reversion loss [4], but the additional chip area for extra power MOSFETs and their control circuity, as well as additional capacitors, are steep prices to be paid.

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whereas the bulks of all NMOSFETs are connected to the ground. All power MOSFETs (M1–M8) are controlled by two out-of-phase clock signals, i.e., $P_1$ and $P_2$, and their complements, $\overline{P}_1$ and $\overline{P}_2$. Transistors M5–M8 are controlled by the clock signals directly, whereas M1–M4 are switched on and off by node voltages $N5$ and $N6$, which are indirectly controlled by the clock signals through flying capacitors $C_{F1}$ and $C_{F2}$.

Since the structure of the CCVD is perfectly symmetrical, its operation can also be analyzed separately for the left- and right-hand sides. In fact, CCVD can be treated as a pair of voltage doublers operating in opposite states. For instance, when the voltage doubler on the left (which consisted of M1, M3, M5, M7, and $C_{F1}$) is in its charging phase, the one on the right (which consisted of M2, M4, M6, M8, and $C_{F2}$) is in its discharge phase. In this phase, $P_1 = \overline{P}_1 = 0$ V and $P_2 = \overline{P}_2 = V_{IN}$. On the left-hand side, M5 is turned off while M7 is turned on; therefore, node N3 is connected to the ground. The gate voltage of M1 (i.e., $N6$) is supplied by flying capacitor $C_{F1}$, which is about $2V_{IN}$. As a result, M1 would be turned on and $C_{F1}$ would be charged to $V_{IN}$. At the same time, M3 is turned off to prevent $C_{F1}$ to be connected to $V_{OUT}$. Conversely, M6 is on and M8 is off for the right-hand side, connecting node $N4$ to $V_{IN}$ accordingly. Since $C_{F2}$ is charged to $V_{IN}$ in the previous phase, the connection of node $N4$ to $V_{IN}$ would pump node $N6$ to $2V_{IN}$, thus controlling M1 and M3 as just explained. Simultaneously, M2 is turned off and M4 is turned on, connecting the voltage of $2V_{IN}$ to $V_{OUT}$ and discharging $C_{F2}$ to the load in the process.

### B. During Normal Dead-Time Period

In order to prevent the short-circuit currents flowing directly from $V_{IN}$ to ground through M5 and M7 or through M6 and M8 when the phase is switching, nonoverlapping clocks are applied to M5–M8 in practice [1]. The period in which M5–M8 are all switched off ($P_1 = P_2 = 0$ V) is called the dead-time period. The circuit condition during this period is shown in Fig. 2(a). It is shown that transistors M5–M8 are all shut off to prevent short-circuit current loss. However, since the flying capacitors are now floating, there is no control of the node voltages for the transistors, which are depicted in Fig. 2(a). As a result, there are currents flowing from the output capacitor $C_O$ back to the flying capacitors ($C_{F1}$ and $C_{F2}$) and from the flying capacitors back to the voltage source. These currents are called reversion currents [1], [3], [4] and are shown as black arrows. The reversion currents waste the energy that has been spent for pumping charges from $V_{IN}$ to flying capacitors (and from flying capacitors to output). The charges move back to their original voltage nodes instead of to the load, which would introduce a loss in efficiency called reversion loss. Essentially, the reason of these reversion currents is that the gate voltages of transistors M1–M4 are undefined. Therefore, the MOSFETs cannot be properly switched off and reversion currents occur.

### C. During Modified Dead-Time Period

Intuitively, if the circuit structure is not modified, there is only one alternative control scheme that can be used, in which $P_1$ is substituted by $P_2$, and $\overline{P}_2$ is substituted by $P_1$. By doing so, M1–M4 can be definitively switched on or off, and eliminate the floating condition of the nodes. Fig. 2(b) shows the circuit condition during dead time when all the clock signals are 0 V. On the left-hand side, M5 is turned on and M7 is turned off. As a result, node N3 (the left side of $C_{F1}$) is connected to $V_{IN}$. Since $C_{F1}$ is charged to $V_{IN}$ during the previous charging phase, node N5 (the right side of $C_{F1}$) is now $2V_{IN}$, which can turn on M2 and turn off M4 properly. The same condition is applied to the right-hand side transistors M6 and M8, thus making sure M1 is on and M3 is off. Although this approach can eliminate the reversion currents flowing from $C_O$ back to the flying capacitors, there are still reversion currents flowing from $C_{F1}$ and $C_{F2}$ back to $V_{IN}$. Hence, reversion currents cannot be completely eliminated under this control scheme. If all the clock signals are connected to $V_{IN}$ instead, the situation is similar and is shown in Fig. 2(c). M5 and M6 are turned off while M7 and M8 are turned on. Therefore, nodes N3 and N4 are connected to the ground, effectively making nodes N5 and N6 (the gate voltages of M1–M4) to be $V_{IN}$. Although there is no reversion current flowing from $C_{F1}$ and $C_{F2}$ back to $V_{IN}$, there are still reversion currents flowing from $C_O$ back to $C_{F1}$ and $C_{F2}$. Evidently, reversion loss exists in CCVD cannot be completely eliminated with the conventional circuit structure, due to the intrinsic gate voltages of M1–M4.
The proposed CCVD design is shown in Fig. 3. The bulks of all PMOSFETs are connected to their sources, whereas the bulks of all NMOSFETs are connected to the ground. First-level gate controls are added to a conventional CCVD to apply proper gate control to transistors M1–M4. First-level gate controls, as highlighted in Fig. 3, are essentially CMOS inverters in structure. They have been suggested to be applied to a linear charge pump in [5], where the pumped-up voltage of the next stage was used to drive the gates of the current stage. In the proposed CCVD design, internal nodes of CCVD (i.e., N1–N6) are used for the first-level gate controls, and no extra buffers are required. The added first-level gate controls only occupy 1.2% of the overall chip area. As a result, the chip area and power consumption are conserved at the same time. Two out-of-phase nonoverlapping clocks (P1 and P2) connecting to nodes N1 and N2, respectively, are utilized.

The operations of the proposed CCVD can be explained in Fig. 4, which shows the circuit conditions in different phases. Note that a dead-time period is employed between the charging and discharging phases to enable “break-before-make” mechanism and to improve efficiency by eliminating reversion currents. When the left-hand-side voltage doubler is in its charging phase, the right-hand-side voltage doubler would be in its discharging phase and delivering current to the load, as shown in Fig. 4(a). N1 is connected to \( V_{IN} \), whereas N2 is connected to the ground. Similar to conventional CCVD, M5 is turned off while M7 is turned on in the proposed CCVD; hence, N3 is then connected to the ground. At the same time, the other flying capacitor, \( C_{F2} \), is providing a voltage of \( V_{IN} \) to N6 and to the first-level gate control of M1. The gate control of M1, which is effectively an inverter as highlighted in Fig. 3, now has supply voltages of \( V_{IN} \) (logic low) and \( 2V_{IN} \) (logic high) and an input voltage of \( V_{IN} \) (logic low). This inverter structure will then provide an output of logic high (i.e., \( 2V_{IN} \)) to the gate of M1 to properly turn it on, as in conventional CCVD. Similarly for M2–M4, the first-level gate controls deliver either \( 2V_{IN} \) or 0 V to the gates of the transistors, in the same fashion as in conventional CCVD, to turn on or off the transistors properly and to complete charging of \( C_{F1} \) and discharging of \( C_{F2} \).

After the charging phase, the proposed CCVD enters the dead-time period where both clock signals are 0 V. This is shown in Fig. 4(b). Consider the gate control of M1, which now has supply voltages of 0 V (logic low) and \( 2V_{IN} \) (logic high), and an input of \( 2V_{IN} \) (logic high). Again, the inverter nature of the gate control inverts the input and provides an output of 0 V to M1, completely turning off the transistor. The same situations occur in M2, M3, and M4, completely shutting off the transistors and isolating \( C_{F1} \) and \( C_{F2} \) from \( V_{IN} \) and \( V_{OUT} \). As opposed to conventional CCVD in Fig. 2, there is no reversion current flowing from the charged nodes back to the voltage source in the proposed design, therefore improving overall power efficiency. At the end of the dead-time period, the proposed CCVD resumes normal operation as in conventional CCVD, delivering power on the left and charging flying capacitor on the right, as depicted in Fig. 4(c).

It is worthwhile to investigate the transition from charging/discharging phase to the dead-time period. Previous state-of-art designs may have leakage currents flowing from flying capacitors back to \( V_{IN} \) during this transition [3]. After the charging phase of the left-hand-side voltage doubler in Fig. 4(a), M1 should be switched off and M3 should be maintained in cutoff state for the dead-time period when M5 is being turned on in Fig. 4(b). If M1 is not switched off fast enough when N5 is being pumped to \( 2V_{IN} \), leakage current will flow from \( C_{F1} \) back to \( V_{IN} \) through M1. On the other hand, if M3 is not kept at cutoff during the transition, current may leak from \( C_{F1} \) to \( V_{OUT} \) through M3. Fortunately, it can be shown that the leakage current in the proposed design is negligible under the presented control mechanism. First, it can be seen that by comparing M3 (PMOSFET) in Fig. 4(a) and (b), its source \( V_{OUT} \) and gate N6 voltages during the transition are unchanged and maintained at \( 2V_{IN} \) (i.e., \( V_{SG} = 0 \) V), whereas the drain voltage N5 is changed from \( V_{IN} \) to \( 2V_{IN} \). As a result, M3 will maintain perfectly off. For the case of turning off M1 (NMOSFET), its source voltage is \( V_{IN} \), and drain voltage N5 is increased from \( V_{IN} \) to \( 2V_{IN} \) while the gate voltage is switched from \( 2V_{IN} \) to 0 V. The transient transition is shown in Fig. 5. Although \( V_{DS} \) of M1 is rising (from 0 V to \( V_{IN} \), \( V_{GS} \) is falling at a greater rate (from \( V_{IN} \) to \( -V_{IN} \)) since the switching periods are approximately the same. The NMOSFET will only be on for a tiny fraction of the falling edge of the \( V_{GS} \) when \( V_{GS} \geq V_{THN} \). Moreover, since the source voltage is \( V_{IN} \) where the substrate of the circuit is connected to the ground, there is a body effect that increases \( V_{THN} \) and reduces the amount of leakage. Simulation shows that leakage current occurs for no more than 1.5 ns. The estimated loss due to these leakage currents is at most 4.4% at the worst case scenario (with maximum \( V_{IN} \) and minimum \( I_{LOAD} \)) and less than 0.16% in typical operations. As a result, the leakage currents are insignificant in the proposed design.

IV. MEASUREMENT RESULTS

The proposed CCVD design has been fabricated in 0.35-\( \mu \)m CMOS technology, and the micrograph is shown in Fig. 6. It operates with two flying capacitors of 1 \( \mu \)F each and an
output capacitor of 2 μF at a switching frequency of 200 kHz. It can operate with supply voltage of 0.8–1.6 V, providing output voltage approximately twice of the supply voltage at a maximum loading current of 30 mA. Under $I_{LOAD} = 10$ mA, the final $V_{OUT}$ level with $V_{IN} = 1$ and 1.6 V are 1.958 and 3.171 V, respectively. The measured ripple voltages, including the spikes, are about 10 mV. The measured output waveform at $V_{IN} = 1.6$ V and $I_{LOAD} = 10$ mA is shown in Fig. 7. The efficiency with $V_{IN} = 0.8–1.6$ V at $I_{LOAD} = 10$ mA is shown in Fig. 8.

Note that the threshold voltages of the NMOSFETs and PMOSFETs of the fabricated technology are about 0.59 and $-0.72$ V, respectively. The ability in which the proposed CCVD can operate with a minimum supply voltage of only 0.8 V (80 mV higher than $|V_{THP}|$) is attributed to the simple and highly efficient gate-control mechanism. As shown in Fig. 8,
the measured efficiency of the proposed CCVD is maintained at higher than 90% even when it operates at near-threshold supply voltage. The performance is consistent when $I_{\text{LOAD}}$ is increased to 30 mA under 1- and 1.6-V supply voltages, and the results are shown in Fig. 9. The efficiency is slightly reduced at small $V_{\text{IN}}$ due to the relatively large on-resistance of the MOSFETs under this condition. This effect is more prominent when $I_{\text{LOAD}}$ is increased. Nonetheless, the efficiency of the proposed CCVD is still above 91.5% when $V_{\text{IN}} = 1$ V and $I_{\text{LOAD}} = 30$ mA.

A performance comparison with other state-of-the-art CCVD designs with similar specifications is shown in Table I. It is noted that other designs might have disadvantages in silicon area. For instance, in order to suppress reversion currents in [1], area-consuming high-accuracy resistors are required to control the switch-on time of MOSFETs. The resultant area for the resistors is comparable to eight bonding pads in the technology used [1]. On the other hand, the design in [2] uses two identical CCVDs in parallel; hence, the circuitry and its area on silicon are doubled when compared with a single CCVD. Since its maximum loading current is only 1 mA, the size of the power MOSFETs in [2] is relatively small. If larger amount of $I_{\text{LOAD}}$ is required, the size of the power MOSFETs would have to be increased, not to mention the extra buffers to be implemented. Moreover, the design requires four flying capacitors instead of two, thus increasing the form factor of external components as well. The design in [3] is similar with the proposed design. However, since the level shifters and buffers draw power from the output of the CCVD in [3], the power MOSFETs are designed with greater size to accommodate the increased loading current. According to the micrograph, the power MOSFETs in [3] are larger than those in the proposed design by approximately one-quarter. The additional level shifters and buffers also consume extra area and power. As a result, it can be seen that the proposed design has the smallest area among the designs while power efficiency achieved is also improved due to the elimination of reversion currents and simple circuit structure that further reduces switching loss.

V. CONCLUSION

An area-efficient CCVD with no reversion loss has been presented in this brief. It uses internal nodes to control the power MOSFETs via first-level gate controls so that reversion currents are eliminated. Without the need of extra power MOSFETs, buffers, or external capacitors, the proposed design is simple in structure, cost effective in silicon estate, and excellent in power efficiency. It would be beneficial in modern electronics by saving power and area at the same time.

REFERENCES