Abstract—A power-efficient 90-nm low-dropout regulator (LDO) with multiple small-gain stages is proposed in this paper. The proposed channel-resistance-insensitive small-gain stages provide loop gain enhancements without introducing low-frequency poles before the unity-gain frequency (UGF). As a result, both the loop gain and bandwidth of the LDO are improved, so that the accuracy and response speed of voltage regulation are significantly enhanced. As no on-chip compensation capacitor is required, the active chip area of the LDO is only $72.5 \mu m \times 37.8 \mu m$. Experimental results show that the LDO is capable of providing an output of $0.9$ V with maximum output current of 50 mA from a 1-V supply. The LDO has a quiescent current of 9.3 $\mu$A, and has significantly improvement in line and load transient responses as well as performance in power-supply rejection ratio (PSRR).

Index Terms—Low-dropout regulator (LDO), small-gain stages, nanoscale integrated circuits.

I. INTRODUCTION

Techology scaling has been providing opportunities in low-power high-speed digital and RF designs in the past decades. The shrinkage in device feature size reduces the channel resistances and parasitic capacitances in devices, allows digital processors and transceivers to be operated at ever increasing frequencies [1]–[4]. With the permeation of mobile phones, portable computers and handheld entertainment systems, ubiquitous computing attributed by nanoscale IC technology significantly improves people’s quality of life. Undoubtedly, this technological advancement brings great impacts to analog systems as well. For example, highly energy-efficient power-management circuits are becoming more important due to finite energy sources in portable devices. Moreover, switching noises propagation and signal crosstalk among digital and RF systems may take place via the power lines. To tackle the issue, low-dropout regulators (LDOs) are widely used for voltage regulation and noise suppression, due to the low-noise, ripple-free and fast-transient characteristics [5]–[8]. They are also ideal to be embedded in system-on-chip (SoC) solutions due to their relatively simple structure and few external components.

Consider a LDO with two amplifier stages shown in Fig. 1. The first amplifier is the error amplifier (EA) that amplifies the error between reference and feedback voltages. The second amplifier is a low-gain high-swing output stage (OS) that controls the gate voltage of the power transistor (PT). The LDO has three poles—$p_D$ at the output of the LDO, $p_{EA}$ at the output of the error amplifier and $p_{OS}$ at the output of the high-swing output stage, which are given by $p_D = 1/R_{oPT} C_o$, $p_{EA} = 1/R_{oEA} C_{oEA}$ and $p_{OS} = 1/R_{oOS} C_{oOS}$, where $C_o$ is the output capacitor, and $R_{oEA}$ and $C_{oEA}$ are the output resistance and lumped output capacitance of stage $i$, respectively, for $i = PT$ (power transistor), EA (error amplifier) and OS (output stage). Stability is achieved by cancelling $p_{EA}$ with the zero generated by the equivalent series resistance (ESR) of the output capacitor, given by $z_e = 1/R_e C_o$, where $R_e$ is the ESR of the output capacitor. Moreover, $p_{OS}$ is placed beyond the unity-gain frequency (UGF) of the loop-gain frequency response of the LDO. Both the parasitic capacitances and channel resistances of the transistors are diminished in the nanoscale technology. As the non-dominant poles are shifted to higher frequencies, the constraint on bandwidth is relaxed. However, the reduced channel resistance also lowers the loop gain of the LDO, thus prevents the maximum attainable bandwidth to be achieved, as shown in Fig. 2 [6]. Obviously, the bandwidth of the nanoscale LDO can only be fully extended if the low-frequency loop gain can be improved without affecting the positions of poles and zero.

There are several well developed methods in gain improvement, such as cascoding and gain-boosting [9]–[11]. These approaches rely on increasing the output resistance of an amplifier, and are widely used in sub-micron technology circuits. However, if the gain is increased by applying cascade structure to the error amplifier, $p_{EA}$ is shifted to lower frequency. The pole-zero cancellation must now take place at a lower frequency, too. Either the output capacitance $C_o$ or its ESR $R_e$ has to be increased to shift $z_e$ to lower frequency. If $C_o$ is increased, $p_D$ is also moved to lower frequency which further limits the bandwidth. This contradicts with the advantage of the nanoscale technology, and results in slower responses of the LDO. Moreover, the external component size would be unavoidably increased, which
is undesirable in SoC designs. On the other hand, if \( R_e \) is increased, the transient responses of the LDO, especially the overshoot and undershoot performances, would be degraded [12]. In either case, improving loop gain actually introduces more design issues.

Another approach to improve the loop gain is by utilizing multiple high-gain stages in the LDO. The loop gain can then be greatly enhanced, but multiple low-frequency poles are inserted. Consequently, internal compensation scheme would be required [6], [8]. Typically, the compensation capacitors required would be in the order of picofarad [8]. Such capacitors would occupy significant portion of die area in the nanoscale LDO. Furthermore, in a power-efficient LDO design where quiescent current is in scarce, the addition of on-chip capacitors may introduce multiple bottlenecks which limit the large-signal performances, for example, the slew-rate behaviour. Certainly, advanced slew-rate enhancement circuits can be employed to solve this problem, but that would make the LDO become more complicated, area-inefficient or even power-hungry. Evidently, simplicity and area are sacrificed in the LDO when the loop gain is increased by this approach.

The paper focuses on investigating a methodology to improve loop gain using multiple small-gain stages. Such stages provides well-controlled gain enhancement without introducing low-frequency poles before UGF. The controllability of gain improvement guarantees the LDO to be stable under large process variations of the technology. As the loop gain is improved, the bandwidth of the nanoscale LDO is also significantly extended. It will be shown that several aspects of the LDO performance are improved as a result. The design of the proposed channel-resistance-insensitive small-gain stages would be discussed in the next section. Analysis and simulation of the proposed LDO utilizing the small-gain stages are presented next. Finally, experimental results and conclusion will be given.

II. DESIGN OF PROPOSED CHANNEL-RESISTANCE-INSENSITIVE SMALL-GAIN STAGES

A. Proposed Channel-Resistance-Insensitive Small-Gain Stage

A design of small-gain stage is proposed in order to generate a channel-resistance-insensitive voltage gain. The circuit structure is shown in Fig. 3. The size of \( M_A \) is \( k \) times that of \( M_B \) (i.e., \( (W/L)_A = (W/L)_B \)), and their total bias current is \((k + 1)I_B\). As a result, \( M_A \) has \( kI_B \) of drain current while \( M_B \) has \( I_B \). It is noted that \( V_{SDA} \) equals \( V_{SDB} \) by connection, and \( \lambda \) is constant for a particular technology with a fixed channel length [13]. As a result, the transconductances of the transistors are given as

\[
g_{mA} = \sqrt{2I_{SDA}h_{p}C_{OX} \left( \frac{W}{L} \right)_{A} (1 + \lambda pV_{SDB})} \\
g_{mA} = \sqrt{2(kI_{SDB})h_{p}C_{OX} \left[ \frac{k}{(W/L)_{B}} \right] (1 + \lambda pV_{SDB})} \\
g_{mA} = k\lambda pV_{SDB} \tag{1}
\]

where \( g_{mA} \) and \( g_{mB} \) are the transconductances of the transistors \( M_A \) and \( M_B \), respectively. Note that they are independent of supply conditions as well as device output resistances. Consequently, the low-frequency gain of the small-gain stage is given by

\[
A_0 = \frac{V_o}{V_{in}} \\
= -g_{mA} \times \left( \frac{\tau_{A0}A_{0}B_{0}T_{0}N}{g_{mB}A_{0}B_{0}T_{0}N + \tau_{A0}A_{0}B_{0} + \tau_{A0}A_{0}N + \tau_{B0}B_{0}N} \right) \\
= -k \left( \frac{g_{mB}A_{0}B_{0}T_{0}N}{g_{mB}A_{0}B_{0}T_{0}N + \tau_{A0}A_{0}B_{0} + \tau_{A0}A_{0}N + \tau_{B0}B_{0}N} \right) \tag{2}
\]

where \( \tau_{A0}, \tau_{A0} \) and \( \tau_{B0} \) are the channel resistances of transistors \( M_B, M_A \) and \( M_B \), respectively. There are two major observations in the expression:

1. The magnitude of the gain is bounded by the ratio \( k \) (i.e., \( |A_0| \leq k \)).
2. The low-frequency voltage gain, \( A_0 \), is only weakly affected by channel resistances.

Even though the channel resistances of the devices can be unpredictable in nanoscale technology, their values are relatively irrelevant in generating the gain. Variation in channel resistances, in turn, only affects the accuracy of the actual gain to the ratio \( k \), but would never cause the gain to shoot up to an unexpected level. Thus, this technique provides robustness amid heavy process variations in nanoscale technology.

The transfer function of the proposed single small-gain stage is given by

\[
A(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{A_0 \left( 1 - s C_{SDB} \frac{g_{mA}}{g_{mB}} \right)}{1 + s \left( \frac{\tau_{A0}A_{0}B_{0}T_{0}N + \tau_{A0}A_{0}B_{0} + \tau_{A0}A_{0}N + \tau_{B0}B_{0}N}{g_{mB}A_{0}B_{0}T_{0}N + \tau_{A0}A_{0}B_{0} + \tau_{A0}A_{0}N + \tau_{B0}B_{0}N} \right) C_1 \tag{3}
\]
where $A_0$ is the low-frequency gain given by (2), $C_{gdA}$ and $C_1$ are the gate-to-drain capacitance of transistor $M_A$ and the lumped output parasitic capacitance, respectively. The pole is located at very high frequency since both the equivalent output resistance and the parasitic capacitance are small, and the zero is at even higher frequency. The small-gain stage with different values of $k$ are simulated with BSIM4 models of UMC 90-nm CMOS technology and shown in Fig. 4, with $I_B = 0.8 \mu A$. First of all, it can be observed that the gain is roughly close to the multiplication factor $k$. However, when the value of $k$ is increased, the actual gain deviates from the expected factor more significantly, due to the further reduced value of $r_{OA}$ as the channel width of $M_A$ is increased. It is noted that the magnitude drop due to the pole levels off at very high frequency, because of the effect of the right-half-plane (RHP) zero. However, its effect is irrelevant since it takes place outside the frequency band of interest. Nonetheless, the gain remains constant throughout the wide bandwidth of the amplifier, regardless the actual value of the gain. It is noticed that when the multiplication factor $k$ is getting large, much more current is consumed but the gain is only increased very slightly. As a result, the next section will introduce a power-efficient methodology to increase the gain.

### B. Cascade Structure of Multiple Small-Gain Stages

Although gain improvement can be done using a single small-gain stage, it would be more efficient in power if it is achieved using cascade structure of multiple small-gain stages. For instance, in order to produce a theoretical gain of $k^2$ using a single proposed small-gain stage, a branch of current bias with value of $(k^2 + 1)I_B$ would be needed. However, it can also be achieved by utilizing multiple small-gain stages to reduce current consumption effectively. For example, if a multiplication of gain of 16 is desired, a single small-gain stage would require $(16 + 1)I_B = 17I_B$ but two small-gain stages would only need $2 \times (4 + 1)I_B = 10I_B$. Moreover, by utilizing multiple stages, each stage is only required to contribute a smaller portion of the gain. Hence, the gain degradation caused by the increasing value of each $k$ is relieved. Consequently, by reducing the multiplication values of each stage, the parasitic gate capacitance at each stage input is kept small, thus ensuring all poles are placed at sufficiently high frequencies. A cascade structure of two small-gain stages is shown in Fig. 5. For simplicity, $k_1$ is designed to be equal to $k_2$, so that $M_{1A}$ and $M_{2A}$ are of the same size, as well as $M_{1B}$ and $M_{2B}$. The transfer function of the two-small-gain-stage amplifier is given by

$$A(s) = \frac{v_o(s)}{v_{in}(s)} \approx \frac{g_{mA}^2 R_1 R_2 \left(1 - s \frac{C_{gdA}}{g_{mA}}\right)^2}{(1 + s g_{mA} R_1 R_2 C_{gdA} + s^2 R_1 R_2 C_1 C_2)}$$

(4)

where $g_{mA}$ and $C_{gdA}$ are the transconductance and gate-to-drain capacitance of transistor $M_{1A}$ (or $M_{2A}$), respectively, and $R_i$ and $C_i$ are the equivalent resistance and lumped capacitance seen at the output of stage $i$ (for $i = 1$ and 2), respectively. It can be approximated to the following if the Miller-multiplied capacitance is significantly larger than the lumped output capacitances:

$$H(s) \approx \frac{g_{mA}^2 R_1 R_2 \left(1 - s \frac{C_{gdA}}{g_{mA}}\right)^2}{(1 + s g_{mA} R_1 R_2 C_{gdA} + s^2 R_1 R_2 C_1 C_2)}.$$  

(5)

The non-dominant pole and zeros can be easily placed beyond UGF, while the dominant pole is dependent on the size of transistor $M_{1A}$ (and $M_{2A}$). As in the case of single small-gain stage, the zeros here are located well beyond the pole locations. The two-small-gain-stage amplifier is simulated and the result is shown in Fig. 6. The designed voltage gain is the same as the one in the previous section with $I_B = 0.8 \mu A$, but is separated into two small-gain stages equally (i.e., $k_1 = k_2 = \sqrt{k}$). Comparing to Fig. 4, the gain of two-stage amplifier is much closer to the designed value than that of single-stage amplifier,

Fig. 4. Simulated frequency response of the proposed small-gain stage with different multiplication factor $k$.  

[Image of magnitude plot with log-log axes and data points for $k = 4, 8, 16, 36, 64, 100$.]
while current consumption is significantly reduced. The increased gain is also stable during the wider range of frequency, since no low-frequency poles are introduced. However, it is noted that when $k$ is continued to be increased, $C_1$ and $C_2$ are becoming considerably large. As a result, the complex poles cannot be simply separated, and the approximation of (4) to (5) is no longer valid. The complex-pole frequency is lowered and the damping factor is reduced, which introduce a magnitude peaking at the corner frequency and cause stability issue if that frequency is close to UGF [14]. Therefore, the value of $k$ must be carefully chosen in order to strike a balance between gain, bandwidth and stability.

III. Simulation Results of LDO With Proposed Small-Gain Stages

A. Frequency Response

A LDO incorporating multiple small-gain stages is proposed and shown in Fig. 7. It consists of an error amplifier, three proposed small-gain stages, an output stage and a power pMOS transistor as pass element. Since the designed LDO has a maximum output current of 50 mA, a 1-$\mu$F capacitor is supplied to its output, to provide frequency compensation and to act as charge reservoir when the LDO cannot respond to a sudden load change. The voltage drop at output is given by $\Delta V = I \Delta t / C$, where $I$ is the load current, $\Delta t$ is the response time of the LDO, and $C$ is the output capacitance. Assume the LDO can respond in 1 $\mu$s, the output voltage drop would be 50 mV, which represents the baseline performance. If the LDO can respond faster due to loop-bandwidth enhancement, the transient performance can be improved.

The first small-gain stage is in fact a negative unity-gain buffer (i.e., $k = 1$), which separates the output resistance of the error amplifier and the input capacitance of the next small-gain stage from each other. The gain is then boosted by the two proposed small-gain stages. The signal is passed to the output stage that has a relatively large biasing current in order to reduce its output resistance and to increase its output swing. Since the loop gain of the LDO is enhanced by the proposed small-gain stages, and the threshold voltages of 90-nm transistors are very low, the size of power pMOS transistor is no longer required to be large. The smaller power transistor further reduces its parasitic gate capacitance, thus pushes the associated pole to even higher frequency. Since all
the transistors are very small comparative to the power transistor and the parasitic capacitances of those transistors under 90-nm technology are negligible, the loop gain of the LDO can be expressed as (6), shown at the bottom of the page, where $g_{mi}, R_{oi}, C_{oi}$, and $C_{gdi}$ are the transconductance, equivalent output resistance, lumped output capacitance, and gate-to-drain capacitance of stage $i$, respectively, for $i = E_A$ (error amplifier), $B$ (buffer), $S_1$ (small-gain stage 1), $S_2$ (small-gain stage 2), OS (output stage) and PT (power transistor). $C_o$ and $R_e$ are the output capacitance of the LDO and its ESR, respectively.

There are six left-half-plane (LHP) poles, one LHP zero and one RHP zero, given by $\frac{1}{(R_{dPT}C_o)}, p_1 = \frac{1}{(R_{dPT}C_o)}$, $p_2 = \frac{1}{(R_{dPT}C_oS_1)}, p_3 = \frac{1}{(R_{dPT}C_oS_2)}, p_4 = \frac{1}{(R_{dPT}C_oS_3)}, z_e = \frac{1}{(R_eC_o)}$ and $z_1 = \frac{g_{mPT}}{C_{gdi}R_{dPT}}$. Although there are six LHP poles, the poles generated by the small-gain stages, $p_2, p_3$ and $p_4$, are located in high enough frequency that they would not pose a threat to the stability. Due to the reduced channel resistance and smaller size of the power transistor, the dominant pole is placed in the order of tens of kilohertz. The first non-dominant pole, $p_1$, which is generated at the output stage, is designed to be cancelled by the ESR zero, $z_e$. In order to reduce overshoot and undershoot performances in transient responses, the value of ESR must not be large, which implies the pole-zero cancellation should take place at a relatively high frequency. As a result, the output stage is designed to have more bias current to lower its output resistance to push $p_1$ to the order of megahertz. The next non-dominant poles, $p_2, p_3$ and $p_4$, are contributed by the small-gain stages. As explained in previous sections, they are placed at a frequency about several tens of megahertz, which are well beyond the designed UGF of 10 MHz and would not introduce stability issues. Finally, the pole contributed by the input stage, is exiled to several hundred megahertz, attributed to diminutive output resistance and insignificant parasitic capacitance. The RHP zero is completely irrelevant within the frequencies of interest, as it is placed at several tens of terahertz. The simulated frequency response of the proposed LDO is shown in Fig. 8, with UGF of 10.3 MHz and phase margin of 41.6°. For comparison, a conventional LDO without the small-gain stages is also simulated and its response is displayed as the dashed line in Fig. 8. The simulation results show that the loop gain is increased by about 20 dB and bandwidth is extended by about 7 times. As the accuracy of the LDO is improved by 10 times, the error can be reduced from, for example, 1% to 0.1%, which is sufficient in most applications. It can also be observed that the phase shifts are the same before 10 MHz in the frequency responses of both LDOs, confirming that no low-frequency poles are introduced. Table 1 demonstrates the variations of UGF and phase margin with respect to output capacitance and its ESR. UGF and phase margin are simulated while the output capacitor is reduced by 10% and the ESR is varied between 90% and 110% of its nominal values. The worse case takes place when the output capacitance is at the minimum and the ESR is at its maximum. However, the phase margin has only been reduced by less than 5%, which would not affect the stability significantly.

Since the accuracy of the LDO is governed by the loop gain and the speed is dominated by the bandwidth, the proposed LDO is expected to have accurate and speedy transient performances. To demonstrate the effects of gain-bandwidth-enhanced LDO, load and line transient behaviours as well as power-supply rejection ratio (PSRR) are investigated.

$$I_L(s) \approx \frac{-g_{mEA}g_{mS1}g_{mS2}g_{mOS}g_{mPT}R_{dPT}R_{dPT}R_{dOS}R_{dOS}R_{dPT}(1 - \frac{C_{gdi}R_{dPT}}{g_{mPT}})}{(1 + sR_{dPT}C_o)(1 + sR_{dPT}C_oS_1)(1 + sR_{dPT}C_oS_2)(1 + sR_{dPT}C_oS_3)\frac{1}{(1 + sR_eC_o)}} \times (1 + sR_eC_o)$$

(6)
B. Load Transient Behaviour

The load regulation of a LDO is defined as the output voltage variation when the load current is changed, and is given by [5], [6]

\[
\frac{\Delta V_O}{\Delta I_O} = \frac{R_{oPT}}{1 + L_0}
\]  

(7)

where \(L_0\) is the low-frequency loop gain of the LDO. As the loop gain is improved in the proposed LDO, its load regulation accuracy should be notably improved. Moreover, since the bandwidth of the LDO is extended as well, its response time should also be shortened. The load transient behaviours of both the proposed and conventional LDOs are simulated. A load current change between 0 A and 50 mA within 10 ns is applied to both LDOs, and the results are shown in Fig. 9. It can be observed that the voltage deviation due to different loadings is smaller in the proposed LDO. Besides, the proposed LDO responds to the change faster than the conventional one, results in smaller voltage spikes in transitions. The simulation results agree with the theoretic analysis, and also show that the proposed LDO is stable even under 10-ns current steps.

C. Line Transient Behaviour

The characteristics of the LDO when the supply line fluctuates is another important metric, and the line regulation is given as [5], [6]

\[
\frac{\Delta V_O}{\Delta V_{IN}} \approx g_{mPT} \frac{R_{oPT}}{L_0} + \frac{1}{\beta} \left( \frac{\Delta V_{REF}}{\Delta V_{IN}} \right)
\]  

(8)

where \(\beta\) is the feedback factor of the LDO. By neglecting the voltage drift due to the reference, the line regulation is inversely proportional to the gain product of the amplifier, similar to the load regulation. The line regulation and line transient behaviour are expected to be drastically improved in the proposed LDO since the loop-gain-bandwidth is significantly improved. The supply voltages for the proposed and conventional LDOs are varied between 1.0 V and 1.2 V (maximum operating voltage of the technology) within 100 ns in simulation. The results are depicted in Fig. 10. The variation due to the supply change is significantly reduced in the proposed LDO. The transient fluctuation also settles faster, due to the improved response speed.

D. Power-Supply Rejection Ratio (PSRR) Performance

Another important characteristic of LDO is the power-supply rejection ratio (PSRR), which describes the ability of LDO to
reject the switching noise or ripples propagated through the supply. At low frequencies up to the UGF of the LDO, the PSRR is dominant by the loop gain and is simply given by [15]

$$\text{PSRR}_0 \approx \frac{1}{L_0}$$  \hspace{1cm} (9)

The simulated PSRRs of both the proposed and conventional LDOs under full current load of 50 mA are shown in Fig. 11. These represent the worse-case PSRRs, since the power transistor is most conductive under full loading current. It can be observed that, the PSRR of the proposed LDO is considerably improved and is about $-56$ dB at low frequencies. As the loop gain of the proposed LDO rolls off at the order of megahertz, the PSRR degrades close to the level of the conventional LDO. The peak in PSRR, indicating the location of the UGF, is also pushed to a higher frequency in the proposed LDO. The PSRR performance is shown to be enhanced by the loop-gain-bandwidth enhancements.

IV. EXPERIMENTAL RESULTS

The proposed LDO has been implemented in UMC 90-nm CMOS technology. The threshold voltages of the nMOS and pMOS transistors in the technology are 0.24 V and $-0.18$ V, respectively. Due to the relatively low threshold voltage, there would still be sufficient overdrive voltage even when the supply
voltage is only 1 V, so that the aspect ratio of the transistor can be lowered. Moreover, since the minimum channel length is reduced, channel width can also be shortened to maintain the required aspect ratio. As a result, the size of the power transistor is only 1500 μm/80 nm. The drawn channel length is 80 nm which is the adjustment defined by the foundry and stated in the design rules. Further area reduction is achieved since the proposed circuit topology does not require any on-chip compensation capacitors. The active silicon area of the LDO is only 72.5 μm x 37.8 μm, and the chip micrograph is shown in Fig. 12. The LDO has a preset output voltage of 0.9 V and maximum output current of 50 mA. It can operate with a minimum supply voltage of 1 V and a quiescent current of 9.3 μA. The output capacitor is 1 μF and its ESR is 0.35 Ω. Measurement results are summarized in Table II.

Fig. 13 shows the load transient response of the proposed LDO. The load current is switched between 0 A and 50 mA in 10 ns. Since both the loop gain and bandwidth of the LDO is enhanced, the LDO is able to react quickly and accurately under load transient situation. The output voltage deviates for only 4.1 mV at maximum loading current. As shown in the zoom-in views in Fig. 14, the overshoot and undershoot are about 8 mV and 6 mV, respectively, and are within ±1% of the final voltage value. It also shows there is only small ringing for the 10-ns load switching. The ringing is suspected to be caused by bondwire inductance.

The measured line transient response is shown in Fig. 15. The supply voltage to the LDO is changed between 1.0 V and 1.2 V in 100 ns, and the output voltage varies for 2.8 mV only. The speedy performance is again due to the improved loop-gain-bandwidth product. The supply voltage is limited to 1.2 V, the maximum operating voltage of the technology, to prevent damages to the devices.

Performance in PSRR of the proposed LDO is measured. The worse-case PSRR, which takes place at full loading current, is depicted in Fig. 16. At low frequencies up to the LDO roll-off frequency at several hundred kilohertz, the achieved PSRR are mostly better than 50 dB. The deterioration of PSRR takes place at higher frequencies in the order of tens of megahertz due to the extended bandwidth. Nonetheless, the proposed LDO attains better than 35 dB PSRR up to 40 MHz.

Table III shows a performance comparison of some previously reported LDOs with the proposed LDO. It is noted that
the proposed LDO has comparatively small load transient deviations, attributed to its significantly improved loop-gain-bandwidth. It is also able to effectively utilize the technology advantage to achieve small quiescent current and small chip area, while providing good regulations and supply-rejection performance with comparable output capacitance.

V. CONCLUSION

This paper presented a low-power nanoscale LDO with multiple small-gain stages to significantly improve both loop gain

<table>
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<th>Table III: Performance Comparison With Previously Published Works</th>
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<tr>
<td><strong>Year</strong></td>
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<tr>
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<td>Dropout Voltage (V)</td>
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<td>Maximum Output Current (mA)</td>
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<td>Quiescent Current, I_Q (µA)</td>
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<tr>
<td>UGF (MHz) @ I_Q(max)</td>
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<td>∆V_O/V_O</td>
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<tr>
<td>Load Regulation (mV/mA)</td>
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<td>PSRR (dB)</td>
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* With the bandgap reference.
and bandwidth. A small-gain stage that is channel-resistance-insensitive is proposed, which separates the relationship between the miniature channel resistance and the amplifier stage gain. This allows the loop gain of LDO to be improved independently, while retaining the advantages of reduced parasitic resistance and capacitance in nanoscale technology. By applying multiple small-gain stages to a LDO with a power-efficient methodology, the accuracy and speed of the LDO are significantly enhanced. Moreover, analysis of the proposed LDO revealed that the no low-frequency poles are introduced. Both simulation and experimental results confirm that the load transient, line transient and PSRR are improved as results from the loop-gain-bandwidth improvement. The overshoots and undershoots in transient responses of the LDO are also improved, attributed to a smaller value of required ESR of the bypass capacitor for pole-zero cancellation. Consequently, the nanoscale LDO is faster and more accurate. Moreover, the circuit topology eliminates the need of on-chip compensation capacitors, thus saves much fabrication area. The performances are especially encouraging with the low quiescent current.

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REFERENCES


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